AC BOX DOCUMENTATION

1. INTRODUCTION

The purpose of this document is to consolidate the information we have about our computer controlled AC signal generators. It should help to recognize the major parts in the AC box and understand roughly how they work. These AC boxes provide two pairs of outputs (Chan.1 and Chan 0) . Each pair produces a user adjustable sine-wave with tunable frequency and phase. The signals that comprise each pair are 90 degrees out of phase. (i.e. chan 1x 1y, chan 0x 0y)

2. OPTOISOLATOR BOARD

The optoisolator board has two main functions. The first is to output a clock signal from a reference oscillator operating at around 30 MHz to the two analog devices direct digital synthesizers (DDS). The second is to pass seven digital control signals to both boards. Both reset signals and the update signal are shared by both DDS cards.

We talk to the AD9854 cards using the NI-6501 USB interface which has the following pinouts:

- PA6 → "Pre-update"
- PA5 → “IO RESET”
- PA4 → “SI1”
- PA3 → “SI2”
- PA2 → “SCLK1”
- PA1 → “SCLK2”
- PA0 → ”MASTER RESET”

Each signal passes through an optoisolator before being routed to the two DDS cards. See Ben’s schematic of the PCM 1704 box on the private wiki for correct connector mapping of PA6 to PA0. The optoisolators (4N35) have a small LED inside connected to pins 1 and 2 (pin 3 floats). Pin 1 is pulled up to the digital 5 volt supply. Pin 2 is the input, given through a 400 Ohm current limiting resistor. When the input is low, the light shines and pulls the output of the phototransistor (pin 4) to ground. When then input is high, the light stops shining and the output is pulled up to +3.3 volts (there is a 10k resistor from pin 5 to to +3.3V). Pin 5 is connected in ground, and pin 6 floats. See the wiki for a schematic diagram of the optoboard.

3. POWER SUPPLY BOARDS

There are two main DC voltage levels required by the box. +5 volts to power the clock/hex inverters on the optoboard and +3.3 volts for each DDS card. The +3.3 volt
regulated supplies are generated by three boards which have three-terminal regulators on them. These are simply integrated circuits that provide a stable low-ripple DC voltage from the +5 V unregulated DC from the transformers that you see inside. They have a built in voltage reference, and you can adjust the output voltage by turning the trimmer pot with a small screwdriver. Make sure not to exceed about 3.4 volts.

4. DIRECT DIGITAL SYNTHESIZER CARDS

4.1. inputs and pinouts.

(1) Serial Clock: SCLK 1 and 2 → “WRB” (DDS card registers data on rising edge)
(2) Serial I/O: SI 1 and 2 → “A0” (Serial Input Output Line)
(3) IORESET → “A2” (Reset Serial Comm.)
(4) MRESET → “MRESET” (Master reset for DDS card).
(5) Update: → “IO UD” (Data transferred from buffer on update high)

4.2. Principle of Operation. The DDS card works by implementing a counter and a lookup table (among many other things, but this is the bare essence). You have to supply an input number M, and on each clock cycle a circuit-block called the phase accumulator adds M to its current value. This phase gets translated to the appropriate part of the sin wave in a phase/amplitude converter circuit. When \( M = 1 \) it will take \( 2^N \) steps to go through the phase accumulator. This corresponds to the lower-limit of output frequency (it will take \( 2^N \) clock periods to generate one period of the output sin wave). If \( M = 2^{N-1} \) the highest possible frequency is attained. At the last stage, a D/A converter generates an analog output. To change the phase of the output, the user simply adds a constant offset to the phase accumulator (in addition to M). The setup is shown in figure 1, and a diagram for understanding the phase-accumulator in figure 2.
Figure 1. Taken from [1]: On every rising clock edge, the phase accumulator adds $M$ to its current value. The phase accumulator is a modulo $N$ counter, so it will overflow and reset.

Figure 2. Taken from [1]: On each clock cycle, the arrow in the phase accumulator increments by $M$ steps.
The system clock is generated by multiplying the input reference clock frequency by a user-programmed integer between 4 and 20. It is also possible to provide a 300 MHz reference directly.

4.3. **Synchronization.** To use two DDS cards together to provide a fixed phase offset, it is necessary to operate off of the same reference clock. In addition each device must be reset and updated simultaneously. The layout of our boxes goes somewhat like the figure below.

![Diagram](image)

**Figure 3.** Taken from [2]: On each clock cycle, the arrow in the phase accumulator increments by M steps

Note that the DAC outputs are 50 Ohm terminated, and have a safe voltage range of -.5 to 1 volt.

**References**

[2] Analog Devices *Synchronizing Multiple AD9852 DDS-Based Synthesizers* By David Brandon