

Single electron capacitance spectroscopy of vertical quantum dots using a single electron transistor.

by
Michael Koltonyuk

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ABSTRACT

We have incorporated an aluminum single electron transistor (SET) directly on top of a vertical quantum dot, enabling the use of the SET as an extremely responsive electrometer to the movement of charge in the dot. This permits high sensitivity probing of single electron addition spectrum of the dot. Signals are modulated by variation in SET response. We demodulate the observed signal using two methods. Capacitance peaks resulting from electrons tunneling into discrete quantum levels are extracted separately for each method, producing closely similar results.

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Introduction

The single electron transistor (SET)^{1,2,3} is a highly charge-sensitive device, capable of detecting charges far less than that of one electron. This remarkable property allows an SET to be used as an extremely responsive electrometer, making it a very useful tool in experiments where such unique sensitivity is required. While practical applications of SET still remain challenging⁴, some experiments in the past succeeded in exploiting SET's unique properties^{5,6}. Here, we describe a novel method for using an SET as a charge sensor to study electron addition spectra of a quantum dot.

A quantum dot or (sometimes called an 'artificial atom') is a small region of space defined in a semiconductor material with a size of order 100 nm⁷. Each dot is made out of roughly a million of atoms together with an appropriate number of tightly bound electrons. However, a dot can also contain a small number of free electrons, which we can vary at will. Just like in a real atom, these electrons are attracted to a central location being trapped in a bowl-like parabolic potential well. Because the well's dimensions are so small, at sufficiently low operating temperatures electrons occupy quantized energy levels, and thus have a discrete excitation spectrum. Measurements of the orbital energies in these 'atoms' allows us to probe directly many important laws of quantum mechanics. A large number of experimental techniques have proved successful in such measurements⁸. One of them is based on the fact that when an electron enters or leaves the quantum dot, it leads to a noticeable change in dot's capacitance, which can be detected using, among other options, an SET. Single-electron capacitance spectroscopy performed with conventional FETs has permitted measurement of a few thousand

electron additions in a single dot, starting from the first one⁹. The novelty of our approach consists of positioning our SET directly on top of the dot and thus closer to it as opposed to a lateral arrangement used previously¹⁰, thereby creating a possibility for a higher experimental sensitivity and lower noise. Using an SET as a spectroscopic probe of the dot's quantum states allows us to minimize the feedback of our electrometer on the dot so as not to diminish experimental resolution and push operating temperatures below those that are easily obtainable. This arrangement is well suited for detecting any motion of charge under material's surface, and it is flexible enough to allow study of charge motion in defects and impurities as well as a number of quantum dot structures.

Chapter 1

SET Principles¹¹

Coulomb blockade

The single-electron transistor derives its name from the fact that transferring a single electron through it has a measurable effect. The operation of the SET is based on the Coulomb blockade principle^{1,12}. The electrons flow through this device as separate entities, with the total current limited by a potential barrier determined by the electrostatics of the system.

The SET consists of a metal island coupled to the source and drain electrodes through two small tunnel junctions. A diagram of the SET structure is shown in Figure 1.

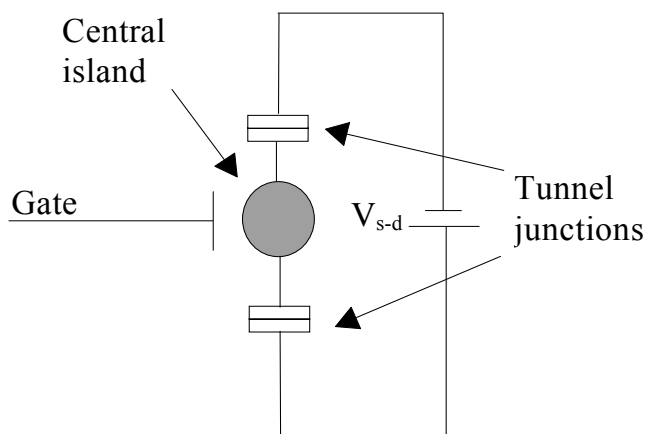


Figure 1. Schematic of a Single-Electron Transistor.

Let's consider the tunneling process in detail. To traverse the device from source to drain, the electrons must jump onto the center island through one of the tunnel junctions and then jump off through the other. In this process, the charge on the capacitance of the central island must change by the quantized amount e . The center island capacitance, C , is the sum of all the capacitances of the central island to its environment. The energy required to charge the capacitance of the central island by one electron is equal to $E_c = e^2/2C$ and is referred to as the charging energy. To travel from source to drain, the electrons must possess sufficient energy to overcome this potential barrier.

The charging energy becomes important when it exceeds the thermal energy, $k_B T$. Then, the electrons cannot be thermally excited over this energy barrier. Ideally, for a zero source-drain voltage bias, the current through the device is zero and the number of electrons on the central island is fixed. Of course, in a real situation, the precision of the above discussion is limited mainly by co-tunneling events and finite temperature effects^{13,14}.

Since we are dealing with ultra-small structures, a possibility exists that the Heisenberg uncertainty relation might invalidate the described above process. Given that $\Delta E \Delta t = (e^2 / C) R_T > h$, the tunnel resistance R_T must be much larger than $h/e^2 = 26 k\Omega$. Otherwise, the charge on the central island is not well-defined because the wavefunctions of electrons are localized there sufficiently. In this case, quantum fluctuations can destroy the quantization of charge in Coulomb blockade.

The condition $E_c = e^2/2C \gg k_B T$ is satisfied for low temperatures and a low central island capacitance. For an SET located away from other metallic objects,

capacitances of the tunnel junctions make up a significant contribution to C , and in a typical SET have areas of about $70 \times 70 \text{ nm}^2$, each with a capacitance of about 80 aF ($80 \times 10^{-18} \text{ F}$). Thus, typically, C is about 200 aF , with a charging energy of 0.4 meV . A scanning-electron photograph of an aluminum SET fabricated with the double-angle evaporation method is shown in Figure 2. The gate electrode is located in this case below the central island and is therefore invisible. This fabrication method is described in Chapter 3. The minimum operating temperature for a SET with these parameters is about 1 K .

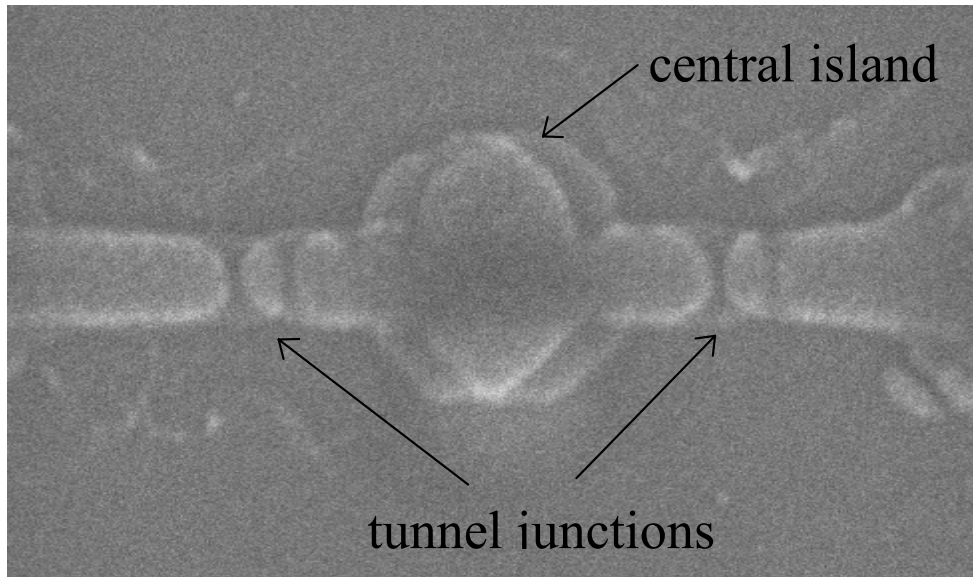


Figure 2. A scanning-electron photograph of an aluminum SET fabricated with the double-angle evaporation method.

Each tunneling electron changes the electrostatic energy of the central island by a discrete value. By applying voltage V_g to a gate electrode that is coupled to the SET central island through a capacitance C_g , we have a way to alter that energy in a smooth

manner. The gate voltage induces an effective continuous charge $Q = C_g V_g$ on the central island, whose energy now becomes:

$$E(n) = \frac{(Q - ne)^2}{2C},$$

when n electrons are present there. If $Q = (n + 0.5)e$, the electrostatic energies corresponding to n and $n+1$ are equal. Here, the number of electrons on the SET central island can change from n to $n+1$ since the two states have equal probability of occurrence. Thus, as we sweep V_g , the build up of polarized charge would be compensated by periodic tunneling of discrete electrons onto the central island. As a result, finite current can flow through the device at these points in gate voltage, because as an electron tunnels onto the central island, the number of electrons on the central island goes from n to $n+1$. Then, as the electron tunnels off the central island, the number of electrons on the island goes back to n .

Energy diagrams

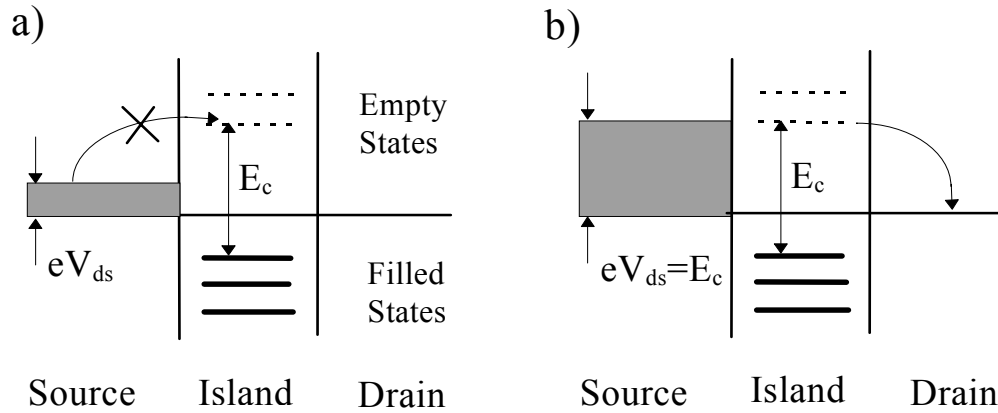


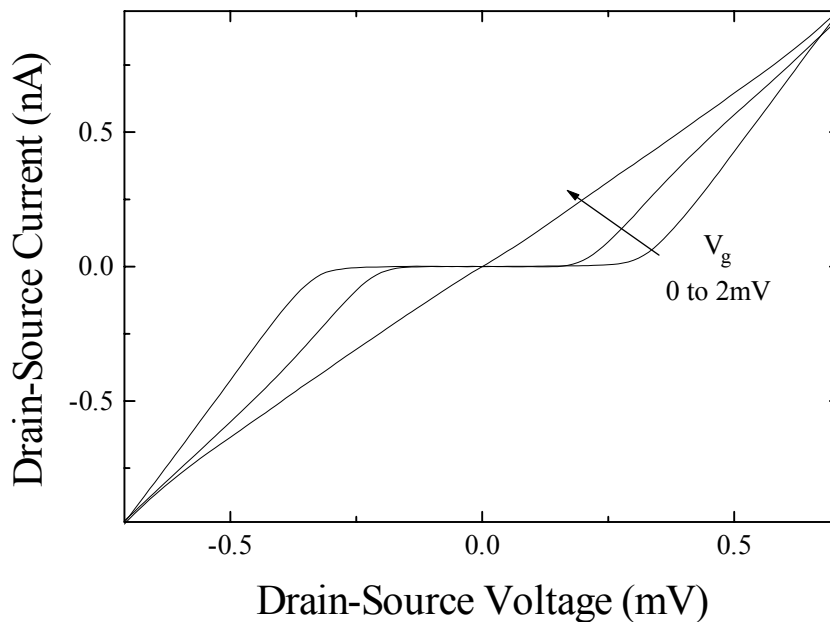
Figure 3. Energy diagrams of Coulomb blockade. a) Coulomb blockade condition - current is zero. b) The drain-source voltage bias is enough to overcome the charging energy barrier.

The Coulomb blockade principle can be further illustrated in the energy level diagrams in Figure 3. Figure 3a depicts the situation where the source-drain voltage bias is small and electrons cannot overcome the energy barrier, resulting in a zero current. Here, current flows through the device only when V_g is adjusted to align the energy levels on the central island with the Fermi levels in the leads. Figure 3b shows the situation where $eV_{ds} = E_c$. This is the threshold point of conduction through the device for all values of V_g . For larger V_{ds} biases, current through the device is only limited by the resistances of the tunnel junctions.

I-V characteristics

The manifestation of Coulomb blockade in the I_{ds} - V_{ds} characteristics of the single-electron transistor is a region of zero current for a range of small drain-source voltage

biases. The maximum width of the Coulomb blockade region is equal to $2E_c/e$. Figure 4 shows an example of the I_{ds} - V_{ds} relationship of the SET for several gate voltages. Here, E_c is about 0.35meV. The width of the Coulomb Blockade is reduced from $2E_c/e$ to 0 as V_g is increased from 0 to 2mV. At this point, the charge induced on the central island by the gate is $0.5e$ (e is the charge of an electron).



**Figure 4. I_{ds} - V_{ds} of the SET at $T=50\text{mK}$. $V_g=0, 1, 2 \text{ mV}$.
(Courtesy of D. Berman)**

Since the energy levels on the middle electrode are evenly spaced by E_c , the effect of gate voltage is periodic. The data shown in Figure 4 were obtained at a temperature of 50mK. At higher temperatures, the I_{ds} - V_{ds} characteristic becomes more rounded, and finally is completely smeared out above 4K.

Gate voltage dependence

Figure 5 shows the dependence of I_{ds} on the gate voltage. The current oscillates periodically, with the period equal to: $P = e/C_g$. Each period corresponds to one electron being added to the central island of the SET. The amplitude of the oscillation depends on the drain source voltage bias. The largest amplitude occurs for $V_{ds} = E_c/e = 0.35mV$.

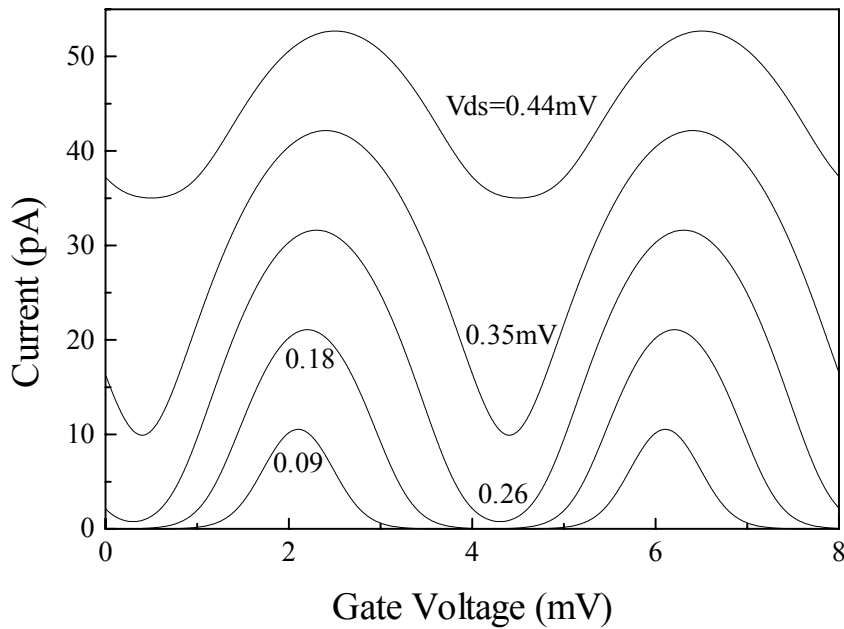


Figure 5. Dependence of the drain-source current on the gate voltage. The largest oscillation occurs for $V_{ds}=0.35mV$

Superconducting SET

Aluminum is a superconducting metal below a critical temperature of $1.18K^{15}$ at zero magnetic field. Since we use the aluminum SETs in experiments below this temperature, we briefly examine their behavior in superconducting state. The physics of

the superconducting SET is rather complex and has been the subject of a great amount of research¹⁶. But, since the goal of our research has been to develop techniques for utilizing the SET as a charge sensor, rather than studying the physics of the superconducting SET, we were mainly interested in the effect of the superconducting properties of the SET on our charge measurement experiments.

The maximum voltage width of the zero current region of a superconducting SET is much larger than it is in the normal state. This width is $(4\Delta + E_c)/e$, where $\Delta = 0.18\text{meV}$ is the superconducting gap of aluminum¹⁵, and E_c is the charging energy of the SET in the normal state. As with bulk aluminum metal, the superconducting properties of the aluminum SET are suppressed by applying a magnetic field through the sample.

Finally, it should be pointed out that the larger maximum voltage width of the zero current region increases the charge sensitivity of the SET in the superconducting state, since the amplitude of the current variation with gate voltage is greater.

Basic operating techniques

We operate the SET in a linear response regime. This means that a small AC signal is applied to the gate of the device. The amplitude of this AC signal is small compared with the period of oscillations, and thus the charge induced is much less than an electron charge on the central island. The response of the SET current to this AC excitation can be expressed as: $I_{SET} = AV_{ac}$. Here, A is the gain, which is proportional to

the slope of the $I_{ds}-V_{gs}$ relationship, shown in Figure 5. Clearly, there are regions of high gain at points where the slope is high, and there are regions of zero gain, at the maxima and minima of the curve. During a charge measurement experiment, it is desirable to bias the charge on the SET at a point of highest slope, but as is shown in Chapter 3, this is not always possible.

The gate electrode is capacitively coupled both to the central island of the SET through a capacitance C_g and to the charge signal through a capacitance C_c . The capacitance of the gate electrode plays an important role in the performance of the SET amplifier. Let's denote the total capacitance of the gate electrode by C_{gt} . This capacitance can be expressed as: $C_{gt}=C_c+C_g+C_{st}+C'$. Here, C' denotes all the stray capacitance that adds to the total capacitance of the gate electrode. Let us also denote the amplitude of the charge signal by Q_s . The fraction of Q_s that appears on the gate electrode is $Q_s C_c / C_{gt}$. The fraction of this charge that appears on the central island of the SET is further reduced by a factor of C_g / C_{gt} . This means that the charge signal is reduced by a factor of $C_c C_g / C_{gt}^2$ by the time it gets to the central island of the SET. If the stray capacitance, C' , is large, this reduction factor could be quite small. In order to make this reduction factor as close to one as possible, C' must be minimized. The largest contributor to C' is the capacitance of J_B , a tunnel junction that is used to bias the DC voltage on the gate electrode. Using a conventional bias resistor would reduce the signal level greatly, because such resistors have stray capacitances on the order of picofarads. This means that the signal from the quantum dot would be reduced by a factor of 10^7 ! The tunnel junction is our solution to this problem, because it has a capacitance of only about 80aF. With these values, the signal reduction factor $C_c C_g / C_{gt}^2$ is about 0.1.

Chapter 2

SET Fabrication¹⁷

Lithography

As described previously, for single-electron transistors to be useful at temperatures easily attained with modern refrigeration techniques ($T=50\text{-}300\text{mK}$), the critical dimensions of these devices must be less than 100nm. Conventional photolithography does not allow faithful reproduction of patterns at such small dimensions. The impeding parameter of this technology is the relatively large wavelength of the radiation used to expose the resist ($\lambda=365\text{nm}$ in most systems available at MIT, $\lambda=193\text{nm}$ in modern photolithography systems used in industry today). When the wavelength of the radiation becomes comparable to the critical dimensions of the pattern, diffraction causes degradation of the pattern fidelity. So generally, the radiation wavelength should be much smaller than the pattern dimensions. One of the available lithographic techniques satisfying this requirement is called electron-beam lithography, which we used to fabricate our devices

We perform the lithography using the beam of a JEOL 6400 scanning-electron microscope (SEM) for transferring the pattern to a resist layer applied to our samples. For pattern generation, we use the Nanometer Pattern Generation System (NPGS) available from Joe Nability Lithography Systems in Bozeman, MT. This system uses a PC with a digital to analog converter card to generate two linear voltage signals. These two voltage signals are fed to the input amplifiers of the X and Y scan coils of the SEM. So

we are able to precisely control the position of the beam with the PC supplying the control signals. In addition, we use a third voltage signal from the PC to control the beam blanking circuit of the SEM to turn the beam off and on as desired.

The pattern is exposed on a point by point basis. Each pattern element written by our system is broken down into “simple” elements, such as boxes, circles and lines. Every element is filled in by scanning the electron beam across its entire area. Usually, the beam is scanned in a serpentine fashion to fill the area of each element. The beam scan is performed by stopping at points spaced apart by a predetermined distance, unblanked for a time period to give every point the proper electron dose, blanked, and then moved on to the next point. Lines of minimal width are written with a single pass of the beam. We were able to obtain features with a minimum linewidth of 60-70nm.

The minimum point to point spacing of the digital-to-analog converter of the computer system is nominally 1.4nm with the field size of $90\mu\text{m}\times 90\mu\text{m}$. The beam diameter of the microscope is about 10nm. This does not mean that we are able to write 10nm wide lines. There are numerous factors that degrade the ultimate pattern resolution of the lithography system. For example, focus drift limits the writing time to less than a few minutes, beyond which the surface of the substrate is no longer in the plane of optimal focus.

The most important factor in electron-beam lithography that limits the pattern linewidth is electron backscattering. As the electrons of the microscope beam impact the surface of the substrate, they scatter backwards into the resist. This effect increases the effective area of exposure in the resist, thus increasing the minimum attainable feature size. Besides obtaining the minimum possible critical dimensions, we need to have a

large undercut in our resist profile, as will be discussed in the following sections. The backscattering process actually helps to increase the amount of undercut. Our solution to this dilemma is to optimize lithography parameters for minimum linewidth, including minimizing the level of backscattering, and to obtain the necessary amount of undercut through other methods, which will be described later in this chapter. The amount of backscattering generally decreases at higher accelerating voltages, so we use the highest voltage available on our electron-beam machine, 40kV. The level of electron backscattering also depends on the substrate material.

Double-angle evaporation

The structure of our single-electron transistor consists of a small metal island coupled to the source and drain electrodes through two metal-insulator-metal (MIM) tunnel junctions. These tunnel junctions are essentially overlaps of two layers of metal with a thin dielectric layer in between. The dielectric has to be thin to allow electrons to tunnel through. The tunneling rate defines the resistance of the tunnel junctions, and is exponentially dependent on the thickness of the dielectric. Since the tunnel-junction resistance is a very important parameter in the operation of our devices, we need to have precise control over the dielectric barrier thickness.

We chose to use aluminum for the fabrication of our devices because it readily forms a smooth, uniform surface oxide layer upon exposure to oxygen gas. The aluminum oxide layer serves as the dielectric tunnel barrier.

Our device structure requires two layers of metal. Traditional planar techniques form multilayer structures in separate lithographic steps. In our case, the bottom metal layer

would be patterned, and then a second lithography would be performed and a second metal layer would be deposited. The dielectric film would be created somewhere in between. Unfortunately, this method is not applicable to our process, because if the first aluminum layer is introduced into the atmosphere after deposition, it is immediately coated with a thick Al_2O_3 layer which is impossible to control precisely. So, as in the original work of Fulton and Dolan², we use the double-angle evaporation technique to fabricate the tunnel junctions. This method allows us to deposit the bottom metal layer, the dielectric layer and the top metal layer in a single vacuum cycle. The dielectric tunnel barrier is deposited in vacuum under controlled conditions and then sealed with another metal layer on top. This way, we are able to accurately control the thickness of the dielectric layer and therefore the resistance of the tunnel junctions.

The double-angle evaporation process is depicted in Figure 1. The aluminum layers are evaporated in an electron-beam evaporator, because its high degree of directionality gives us more control over the patterned metal. The sample is placed inside the thermal evaporator on a tilting stage which can be rotated around an axis with the use of a vacuum feedthrough.

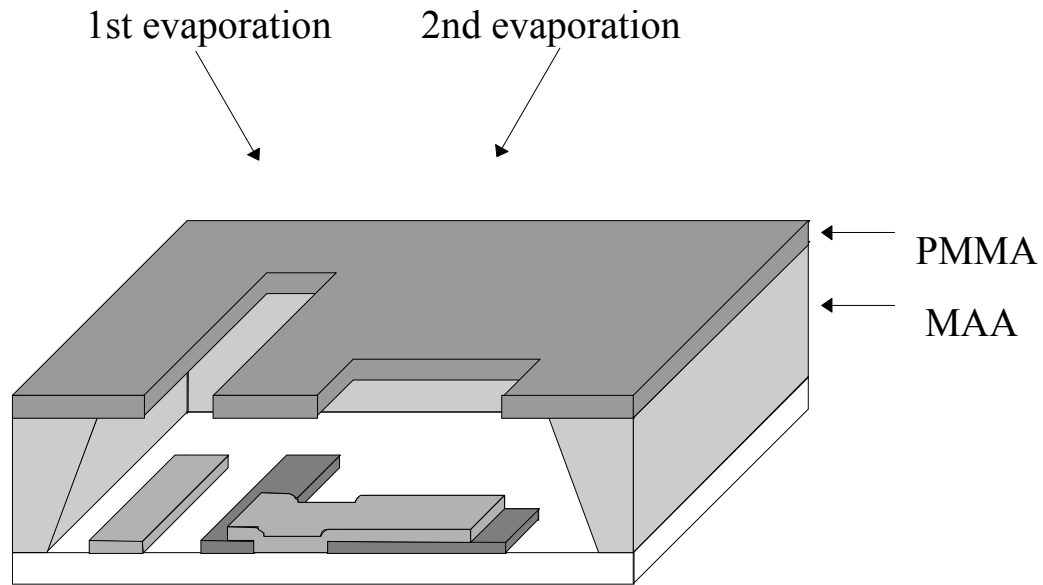


Figure 1. Double-angle evaporation.

For the evaporation of the first layer, the sample is tilted at an angle of -10° . Then an aluminum layer 30nm thick is deposited at a rate of 0.5nm/second. This metal is shown in dark gray on the substrate surface in Figure 1. After a 10 minute cooldown period, the high vacuum valve is closed and 50-100 mTorr of oxygen gas is introduced into the sample chamber. After the aluminum on the substrate is oxidized for 8-12 minutes, the oxygen is pumped out of the chamber. For the second aluminum evaporation, the sample stage is tilted at $+10^\circ$ to the normal. At this angle, an aluminum layer 350 angstroms thick is deposited. This metal is shown as light gray in Figure 1. As a result of the angled evaporations, an overlap is formed between the layers of metal formed in the first and second evaporations. This overlap area is the tunnel junction. The resistance of these tunnel junctions is very repeatable and easily adjustable, because the oxidation is performed in a well-controlled environment.

After the evaporations are completed, the sample is placed in acetone for “lift-off”. The resist is dissolved in the acetone, leaving only the patterned metal on the substrate. Occasionally, we had to place our samples (while submerged in acetone) in an ultrasound vibratory cleaner to achieve a complete “lift-off”.

Resist profile

As a consequence of using a single lithography pattern to perform two evaporations at different angles, the pattern on the substrate surface occupies more area than the pattern on the surface of the resist. To allow for the extra room at the substrate surface, the double-angle evaporation requires a large degree of undercut in the resist profile. To achieve this, we use a bilayer resist structure, as shown in Figure 1. The bottom layer of the resist is a copolymer of poly-methyl-methacrylate (91.5%) and poly-methacrylic acid (8.5%), (PMMA, PMAA), which is 450nm thick. The top layer consists of 950,000 molecular weight poly-methyl-methacrylate (PMMA) which is 50nm thick. This layer serves to define the pattern of the evaporated metal on the substrate.

It is very important to be able to precisely control the degree of undercut in the resist profile. If the undercut is too small, then the sidewalls of the resist may become coated with metal after the angled evaporations. If the undercut is too large, then it is impossible to place two long parallel lines close together, because the resist in the top layer separating the two lines can fall without support in the bottom layer. We found several methods by which we are able to precisely control the undercut in the lower resist layer.

The most dependable method of controlling the resist undercut is UV flood exposure of the bottom resist layer. Immediately after deposition, the bottom resist layer is uniformly exposed with 220nm UV radiation at a power density of $1\text{mW}/\text{cm}^2$ for a controlled period of time (3 minutes). Afterwards, the top resist layer is applied. After exposure, the pattern is developed in a 2:3 solution of methyl-isobutyl ketone (MIBK) : isopropyl alcohol (IPA). The samples are then immediately rinsed in IPA for 30 seconds.

Chapter 3

Quantum Dot Experiment

Vertical quantum dot

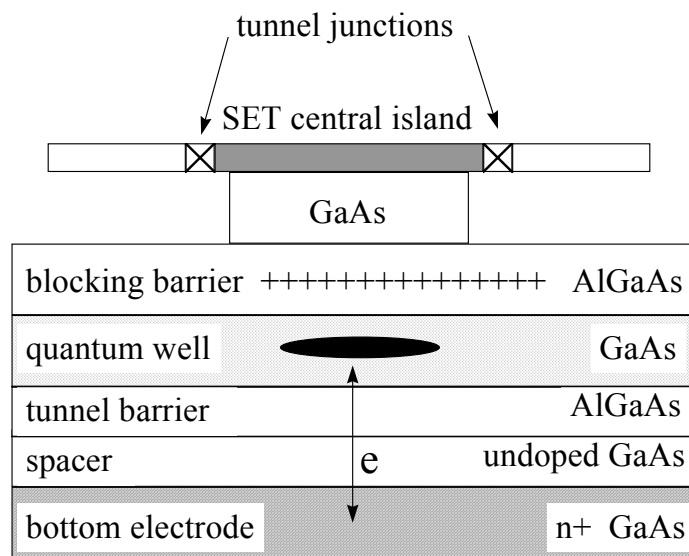


Figure 1. Schematic diagram of the experiment

In our experiment, we study a vertical type quantum dot^{18,19} (Figure 1) confined between two capacitor plates. It is close enough to one of the plates to allow tunneling of electrons from that plate into the dot, but it is far from the other (top) electrode so tunneling from it is prohibited. The sample is fabricated from a GaAs/AlGaAs multilayer wafer grown by molecular beam epitaxy. The layer sequence is as follows: 1- μm undoped GaAs buffer layer; 3500- \AA n^+ ($4 \times 10^{17} \text{ cm}^{-3}$) GaAs bottom electrode; 150- \AA undoped GaAs spacer layer; 85- \AA $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ superlattice tunnel barrier; 150- \AA

GaAs quantum well (vertically confines the quantum dot); 150-Å $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ undoped setback; 350-Å n doped AlGaAs blocking barrier; 300-Å undoped GaAs cap layer.

The spacer layer plays the same role as tunnel junctions for an SET described in Chapter 1. When no voltage is applied to the bottom electrode with respect to the dot, the quantum dot operates in Coulomb blockade regime, so that no electrons can tunnel in or out of it. However, at particular gate voltages (the bottom electrode acts as a gate), it becomes energetically favorable for one more electron to be added to the dot. To coax another electron onto the dot, additional gate voltage is needed.

Sample fabrication

To ensure maximum sensitivity of the SET to charge in the dot, the central island of the SET and the dot must be in close proximity. Our solution to this problem consists of putting the transistor directly on top of a quantum dot. We fabricated the SET on the surface of an MBE grown GaAs/AlGaAs heterostructure using the process described in Chapter 2. This fabrication procedure allowed us to achieve tunnel junctions of the size of about 70×70 nm, with resistance of ~ 50 k Ω and capacitance estimated to be 80×10^{-18} F each²⁰. Then, the central island was used as a mask for wet etching down to the AlGaAs blocking barrier (Figure 1) using $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:8:1000) solution, so as to laterally confine the quantum dot to be directly under our transistor. The etch rate of GaAs in this solution is about 50 nm/min, but varies significantly depending on solution's age. Before the etching, the sample was placed in a UV ozone cleaner for 5 minutes to remove traces of the resist from its surface.

Our sample also contained an ohmic contact to the bottom electrode. By applying voltage on the SET leads with respect to the bottom electrode we control the tunneling of electrons into the quantum dot. Additional surface processing using photolithographic techniques was also necessary to create the gold leads on the sample's surface to which the SET could later be bonded and thus connected our measuring equipment. Since SET is highly static-sensitive, great care had to be taken to keep all of SET's connections shorted together and grounded at all times.

Experimental setup and measurements

The experiment was conducted in a He³ refrigerator at 300 mK. There is no applied magnetic field and therefore the SET is superconducting. We bias the SET as described in Chapter 1 for optimal gain. Then, we apply a DC voltage to the bottom electrode acting as a gate together with a small superimposed AC excitation (20μV rms, 17Hz). The SET current is measured using a current lock-in amplifier. The DC voltage is then slowly varied, and current through the SET is recorded resulting in a signal shown in Figure 2. The frequency of the measurement is sufficiently low so all the signals from the SET are in phase with the AC excitation. The observed in-phase signal is directly proportional to the product of charge induced on the SET central island and $\frac{dI_{SET}}{dQ_{central\ island}}$.

The SET signal exhibits modulation in both frequency and amplitude as evident from our data (Fig. 2a). The fast oscillations are due to a relatively large capacitance linking directly the bottom electrode and the central island. Thus, sweeping the DC voltage induces charge on the SET central island making the bottom electrode act as a gate, so that the SET behaves as shown in Fig. 1e. The period of these oscillations is $P = e/C_{B-S} \approx 275 \mu\text{V}$ ($B-S$ and all other capacitances are defined in Figure 3a), which corresponds to the bottom electrode-to-SET capacitance, C_{B-S} , of $600 \times 10^{-18} \text{ F}$.

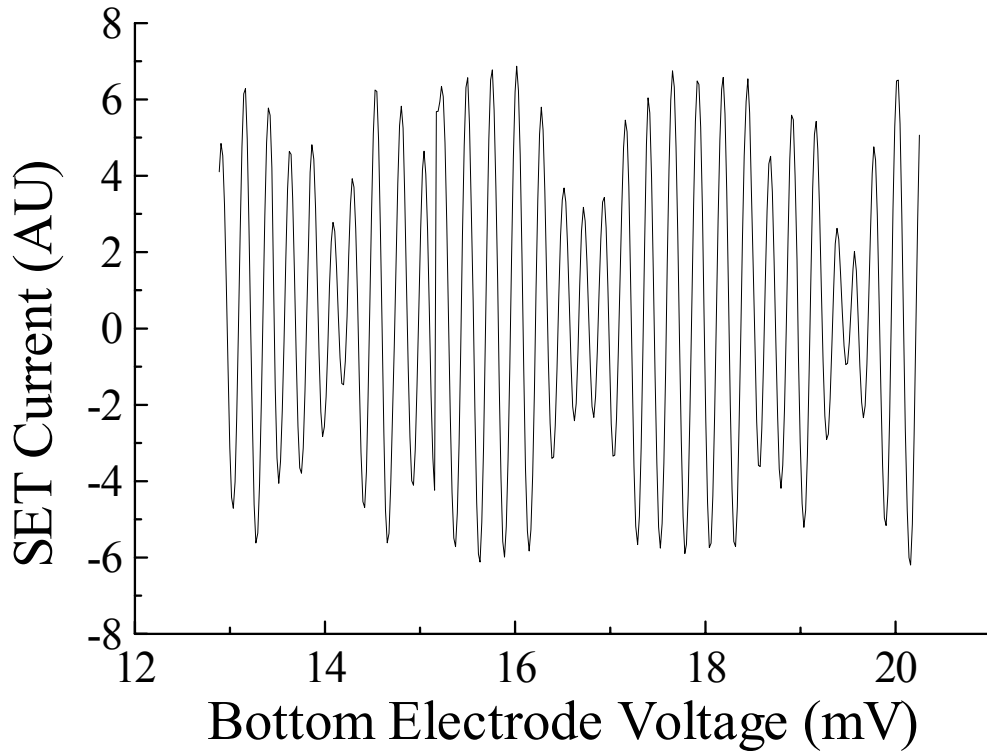


Figure 2. Dependence of the SET current on applied to the bottom electrode voltage.

The overall amplitude of our signal changes noticeably over a period of a few oscillations due to electron addition to the quantum dot (Figure 2). In general, the charge

response, dQ_S , induced on the SET central island by the AC excitation on the bottom electrode (acting as a gate), dV_B , can be expressed as:

$$dQ_S = \left[C_{B-S} + \frac{C_{D-S}}{C_{D-S} + C_{B-D}} \left(C_{B-D} + \frac{dQ_D}{dV_B} \right) \right] dV_B.$$

Here, Q_D is the charge on the dot, Q_S is the charge on the SET central island, and V_B is the voltage on the bottom electrode. The change in current through the SET, dI_S , due to a changing V_B is proportional to the above expression, excluding factors discussed below.

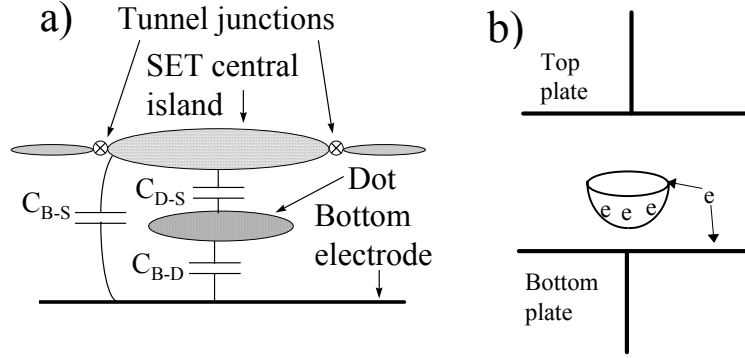


Figure 3. (a) Circuit diagram of the experiment. (b) Schematic diagram of the artificial atom located between two capacitor plates.

Electrons are added to the quantum dot at particular values of V_B , defining a “single electron addition spectrum”¹⁹. Between these values, electron tunneling is not allowed, and dQ_D/dV_B is zero in the above expression. When tunneling does occur and the number of electrons in the quantum dot changes from n to $n \pm 1$, the response of the SET changes drastically because at these points dQ_D/dV_B becomes large. In fact, dQ_D/dV_B behaves as a derivative of a Fermi function, with its peak approaching infinity at zero temperatures.

One might therefore expect that the amplitude of our measured signal, dI_S/dV_B , would increase during tunneling, but in fact the reverse occurs. Because the effective gate capacitance is greatly increased due to the contribution from dQ_D/dV_B , the width of the Coulomb blockade region of the SET shrinks, and so does the SET gain. Also, SET optimal biasing depends on its total capacitance, so that fluctuations in dot's potential cause the transistor to temporarily move away from operating at the point of maximum gain thus providing another reason for diminishing SET current. As electrons enter the dot periodically with gate voltage, the SET current oscillates correspondingly, with one oscillation per electron drawn onto the SET central island. The charging of the dot creates an amplitude modulation in the oscillatory SET response. As electrons enter the dot periodically with gate voltage, the SET current oscillates correspondingly, with one oscillation per electron drawn onto the SET central island. The charging of the dot creates an amplitude modulation in the oscillatory SET response. Because of the much larger effective gate capacitance, fast Coulomb blockade oscillations described above become even faster.

Data analysis and results

To extract the quantum dot capacitance signal from our data, we can exploit either frequency (inverse spacing of oscillations as a function of V_B) or amplitude variation of the SET gain. The frequency of Coulomb blockade oscillations is directly proportional to the charge induced on the SET central island as a result of scanning the potential of the bottom electrode only, and does not depend on the shunting capacitance or any other experimental parameters. Therefore, we can directly extract the quantum dot capacitance

peaks by measuring how the frequency changes when an electron tunnels into the dot, independent of any other experimental variables, such as temperature, biasing of the SET, etc. For this reason we consider this method of extracting the peaks superior to the one based on examination of the amplitude modulation. To minimize background noise, we take a Fourier transform of our data and multiply it by a Gaussian centered around the “carrier” frequency, subsequently taking an inverse transform. We then account for the envelope modulation by scaling all data peaks to unity, so as only phase modulation remains. A frequency modulated sine wave represents this filtered data rather well, so that taking an inverse sine of the modified data reveals the phase change in oscillations due to electrons entering the dot, while the ensuing differentiation produces the desired capacitance peak. The results for two arbitrarily selected electrons entering the dot successively are shown in Figure 4.

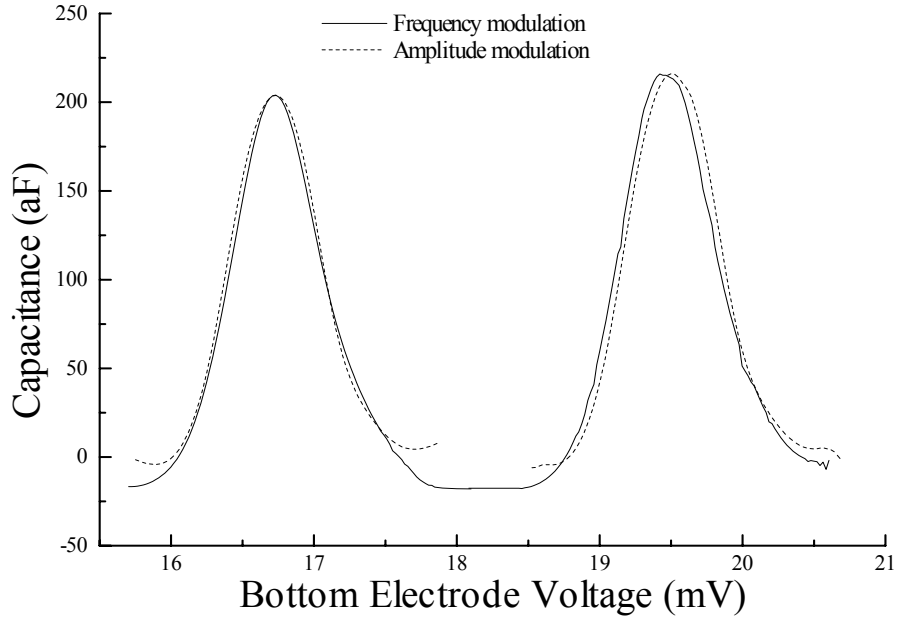


Figure 4. Capacitance peaks of the SET extracted from frequency and amplitude modulation of the measured signal, and corresponding to two electrons entering the quantum dot successively.

Analysis of amplitude modulation of the envelope of the sine wave provides another method for determination of the capacitance. Using a simulation program²¹ designed to calculate analytically the current-voltage characteristic for a system composed of two mesoscopic tunnel junction coupled in series²², we are able to model how the gain of the SET should depend on the additional shunt capacitance due to dQ_D/dV_B . The program is based on the semiclassical model used to describe the two-junction system²³, modified to account for the discreteness of the central island's energy levels. In this model, the state of each junction is fully characterized by the voltage dropped across the junction. The state of the system is then given by V_1 and V_2 , the

voltages dropped across the first and second junctions, respectively. Using charge conservation and Kirchoff's voltage law, we obtain:

$$V_1 = V \frac{C_2}{C_\Sigma} - \frac{ne}{C_\Sigma} + V_g \frac{C_g}{C_\Sigma},$$

$$V_2 = V \frac{C_1 + C_g}{C_\Sigma} - \frac{ne}{C_\Sigma} - V_g \frac{C_g}{C_\Sigma},$$

where C_i is the capacitance of the i th junction, C_g is the gate-SET capacitance, V is the voltage applied to the system, V_g is the voltage applied to the gate, and n is the number of electrons on the central island.

Ensemble-averaged dynamics are obtained from the master equation for $\rho(n, V, t)$ ²², the probability that there are n electrons on the central island at time t with the applied voltage V . In steady state, for fixed V , the net probability of making a transition between any two adjacent states ($n \rightarrow n \pm 1$) must be zero. This simplification together with normalization requirement for ρ allows tunneling rates to be determined at specified temperature, with the resulting current calculated using

$$I = \sum_{n=-\infty}^{\infty} e[r_2(n, V) - l_2(n, V)]\rho(n, V) = \sum_{n=-\infty}^{\infty} e[r_1(n, V) - l_1(n, V)]\rho(n, V).$$

Here, $r_i(n, V)$ and $l_i(n, V)$ are the electron tunneling rates from the right and left, respectively. The I - V characteristic and thus the SET gain may then be calculated if the rates are known as functions of n and V . These rates are easily determined from “golden-rule” calculations²⁴.

We ran the program for several different arbitrarily chosen trial values of that shunt capacitance while keeping all other SET operational parameters (temperature,

tunnel junctions' capacitances and resistances, C_{B-S} , biasing) fixed. The program calculates I-V characteristics for the SET, and from them the gain is determined. Thus, we construct theoretically the relationship between the SET gain and extra shunt capacitance. Then, from our data, we observe how the maximum gain of the SET drops as an electron enters the dot by following the overall envelope of the signal. Subsequently, we apply the reverse transformation relating a drop in gain to an additional shunt capacitance, which we previously have obtained theoretically. Thus, we derive a capacitance peak corresponding to the addition of that electron. Our data displays a decrease in overall amplitude of about a factor of 2, which corresponds to maximum increase in shunt capacitance of approximately 200 aF due to electron tunneling into the quantum dot. A precise determination of the peak amplitude is difficult using this method. The extracted peak height depends critically on the values used in the simulation program for temperature, lead and shunt capacitances. Nonetheless, the determined peak is robust to variations in these data since in the range of our operational parameters the relationship between the gain and the shunt capacitance is nearly linear (Figure 5). (In fact, taking an inverse of the gain drop by itself gives us a good approximation of the capacitance peak.) The capacitance peaks for the same two electrons as mentioned in the previous paragraph are shown in Fig. 4 (re-scaled to fit).

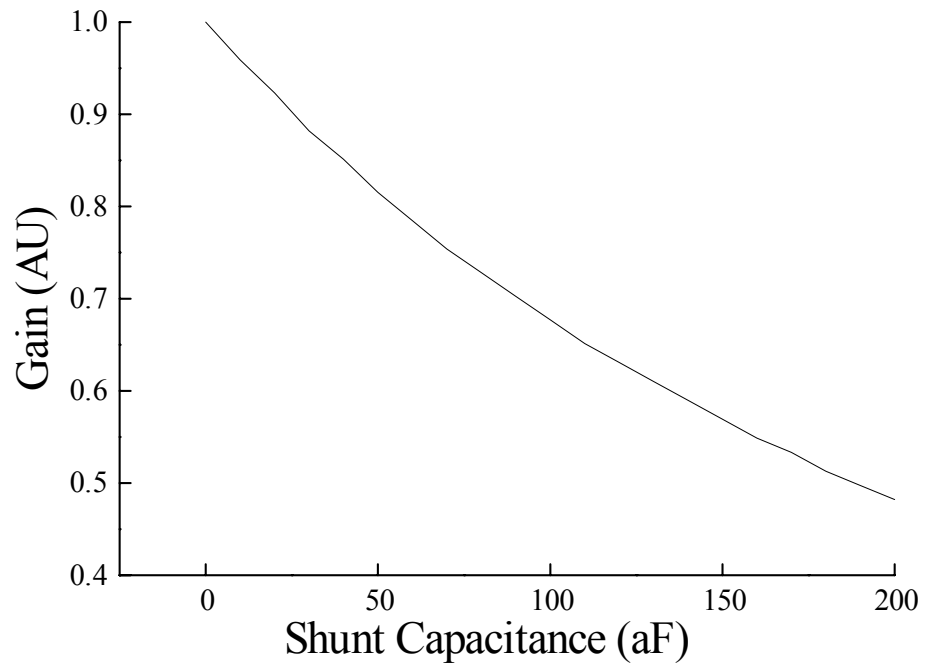


Figure 5. Dependence of the SET gain on additional shunt capacitance due to electron tunneling into the quantum dot.

Conclusion

In summary, we have demonstrated a novel technique allowing an SET to be used as a charge sensor for a quantum dot located directly beneath it and developed two independent methods for interpreting the data. This method holds great potential for applications in other situations, since it allows observing electrons move in a solid with extraordinary sensitivity. The reason we chose such an arrangement was to try to position our SET as close to the dot as geometrically possible, so as to ensure greatest capacitive coupling, which would in turn lead to increased sensitivity of our spectroscopic measurements. However, as it turned out, this design made the SET not only responsive to the charge movement in the dot as we have hoped, but also to the gate – the bottom electrode. In fact, the coupling to the gate is so strong that the signal resulting from it dominates the useful signal from the dot.

There are two potential solutions to this problem that could be investigated further in the future. One way is to try to make the SET coupling to the dot larger by increasing the dot's area. In our experiment, the area of the dot is smaller than that of the SET central island, because etching occurs not only vertically but sideways also, eating away the sides of the dot. Changing the etching procedure could possibly minimize that effect.

Another way would consist of moving the transistor somewhat away from the dot, and using another gate to serve as the top plate of our “capacitor” (the role previously played by the SET). By locating the SET over a depleted region, we can diminish its

coupling to the bottom electrode, and thus perhaps get rid of the fast Coulomb blockade oscillations.

In any case, because this arrangement is so well suited for detecting charge movement under material's surface, it also has a great promise for studying other phenomena, such as defect sources.

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