The Aluminum Single-Electron Transistor for Ultrasensitive Electrometry of Semiconductor Quantum-Confined Systems

by

David Berman

Master of Science, MIT, 1994

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 1998

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Abstract

This thesis describes the implementation of an aluminum single-electron transistor (SET) as a sensor in charge measurement experiments on semiconductor quantum dots. We have used the SET to measure the charge quantization on the quantum dot while varying the strength of the coupling between the dot and the leads. The strength of the coupling has a strong effect on the quantum fluctuations of charge on the quantum dot, which can destroy the Coulomb blockade.

The quantum dot is electrostatically defined with metal gates on top of a GaAs/AlGaAs heterostructure. The patterning of these metal leads and the SET is performed with electron-beam lithography. The technique of double-angle evaporation is used for the fabrication of the SET. The SET functions both as one of the defining gates for the quantum dot and as an electrometer. The capacitively-coupled SET is extremely sensitive to charge on the quantum dot. We control the quantum fluctuations in the dot by varying the conductance of a single tunnel barrier which connects the dot to a charge reservoir. This experimental setup provides us with excellent charge sensitivity and allows us to measure the lineshape with adequate precision to quantitatively compare different theoretical predictions.

Thesis Supervisor: Raymond C. Ashoori
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Acknowledgments

My Ph.D. project took over four years to complete. Throughout this period, there were many people that helped me along the way.

First of all, I would like to thank my family: my parents Liza and Henry Berman and my sister Maria Berman. They provided me with tremendous moral support not only throughout my graduate career, but my entire life. They helped me through the tough times and celebrated my successes with me.

My thesis advisors provided me with lots of useful advice and guidance. Professor Ray Ashoori's energy and excitement gave me the inspiration to dig deeper into the physics of our experiments. His in-depth knowledge and experience helped me gain a better understanding of my experimental results. Professor Hank Smith's experience with nanolithography helped me tackle the numerous obstacles in the fabrication of our devices. Also, his unwavering belief in the ability of an engineer to solve any technical problem inspired me to work harder to overcome the difficulties in my fabrication process.

I am deeply grateful to Dr. Nikolai Zhitenev, a former postdoc in Professor Ashoori's group. In the numerous discussions with him, I got many ideas for my experiments. His constant willingness to discuss physics is greatly appreciated.

I am deeply grateful to Professors Leonid Levitov and Konstantin Matveev for helping me understand the physics of quantum fluctuations of charge on a quantum dot.

Many thanks to Professors Mansour Shayegan of Princeton University and Michael Melloch of Purdue University for providing us with GaAs heterostructure samples for our experiments. I am also grateful to Jack Hergenrother of Harvard University, who helped with his expert advice when I was setting up the electron-beam lithography system in our group.

There are also many fellow graduate students that have helped me. In Professor Ashoori's group, I have had many interesting discussions with Mikhail Brodsky, Ho Bun Chan and Paul Glicofridis. In the Nano-Structures Laboratory, people like David Carter, Juan Ferrera, James Goodberlet, Mike Lim and Tim Savas made it interesting to work alongside them in the cleanroom.

Of course, I would like to thank the technicians in the Nano-Structures Laboratory, Jimmy Carter, Mark Mondol and Jim Daley. They always maintained the equipment and kept it running. When a machine broke, they promptly fixed it.

This work was sponsored by the Office of Naval Research, the National Science Foundation DMR, the David and Lucille Packard Foundation, the Joint Services Electronics Program and DARPA.

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Chapter 1 Introduction

1.1 Charge quantization

The charge on a small isolated puddle of electrons is quantized: it consists of an integer number of electrons. Also, this charge can change only in units of single electrons. For a single electron to jump on or off this puddle, it has to overcome an energy barrier, $E_c = \frac{e^2}{2C_\Sigma}$, which is equivalent to charging a capacitance C_Σ by the charge of a single electron, e. Here, C_Σ is the total capacitance of the puddle to the environment. This effect is referred to as Coulomb Blockade [1-1]. The above description of charge quantization comes with a caveat: the conductance of the tunnel barrier which couples the puddle to the environment has to be much less than $\frac{2e^2}{h}$. Otherwise, the quantization of charge on the puddle is destroyed by quantum fluctuations of charge between the puddle and the environment [1-2]. An alternate description of this effect considers that at conductances larger than $\frac{2e^2}{h}$, the width of the energy levels on the puddle is equal to the spacing between them, and the mean charge on the dot varies continuously with changes in an externally defined potential.

There are several theoretical treatments of the effect of increased tunnel coupling of the dot to the reservoir on the quantization of charge on the dot [1-3][-4][1-5]. The exact

nature of the energy level broadening has only recently been probed experimentally through transport [1-6] and charge [1-7] measurements on the dot. Unfortunately, the exact shape of the energy levels on the quantum dot is difficult to attain with transport measurements. The published data of quantum dot charge measurements [1-7] have had low signal-to-noise ratios, making it difficult to discern whether or not there was good agreement with theoretical calculations.

We have conducted experiments using an aluminum single-electron transistor (SET) to measure charge on a quantum dot with high precision. The techniques that we used in the fabrication of the SET are described in Chapter 2, and the operation of the device is described in Chapter 3. With the single-electron transistor as an electrometer, we have obtained a sensitivity of $1.2\times10^{-3}\,\frac{e}{\sqrt{\mathrm{Hz}}}$ to charge on the quantum dot. The corresponding sensitivity to charge on the gate of the was $6\times10^{-5}\,\frac{e}{\sqrt{\mathrm{Hz}}}$. This value of charge sensitivity is comparable to the record values published in the literature [1-8][1-9].

The charge measurements were performed as we varied the strength of the coupling between the quantum dot and the environment. The high charge sensitivity in our measurements allowed us to compare the data with various theoretical calculations. We found that the theory based on renormalizing the charging energy of the dot [1-5] compare poorly with our data, especially in the regions between the centers of the peaks. The calculations that combine the thermal broadening of the energy levels with a lifetime broadening by convolving a derivative of the Fermi function with a Lorentzian fit our

data better, but there also is discrepancy between the peak centers. Finally, we compared our measurements with calculations based on perturbation theory. These theoretical calculations were performed in two limits. The weak coupling theory [1-3] used the transmission probability through the tunnel barrier coupling the dot to the reservoir as a small parameter in the perturbation calculations. On the other hand, the strong coupling theory [1-4] used the reflection amplitude as a small parameter. We found good agreement between our data and these calculations in both weak and strong coupling limits. These results are presented in Chapter 5.

Aside from the measurements of the energy level broadening of the quantum dot, we have also observed some curious behavior of electrons in some of our samples. Usually, the electrons tunneling onto the quantum dot from a grounded reservoir are attracted by a positive voltage and repelled by a negative one. Sometimes, we observe an opposite response: electrons seem to be repelled by a negative voltage. This effect, referred to as "negative screening" is described in Chapter 6.

1.2 Potential applications of the single-electron transistor

The quantum dot energy level broadening measurements with the aluminum single-electron transistor are an excellent example of the potential usefulness of this device. There are many applications that can benefit greatly from its superb charge sensitivity. For example, experimenters have used a single-electron transistor to create a map of the charge distribution in a Two-Dimensional Electron Gas (2DEG) [1-10]. They fabricated

an SET on the tip of a small tube, which was scanned over the surface of the sample. The current through the SET was significantly modulated by charge in the 2DEG, enabling the measurements to discern variations in the electron density.

Other potential applications of the single-electron transistor can be in data storage. One can imagine quantum dots on the surface of a disk used to store information. An SET fabricated on a probe above the disk can be used to read this information. This application can lead to an enormous data storage density.

Of course, to be useful for commercial applications, the single-electron transistor has to operate at room temperature. Since C_Σ is directly proportional to the surface area of the puddle, it is crucial to use the smallest possible dimensions for single-electronic devices to increase the charging energy. With standard nanolithographic techniques, it is easy to obtain device dimensions on the order of 50-100nm. Generally, such devices operate only at temperatures below 4K, the boiling point of ^{4}He. Thus, many researchers are working towards fabricating SETs, whose maximum operating temperature approaches 300K [1-11][1-12][1-13]. Another beneficial property of these devices is they have been fabricated in silicon with technology that is compatible with the silicon MOS technology used in industry today, although the size of the active area in these devices must be kept on the order of 2nm to increase the operating temperature to 300K.

Most of the proposed room-temperature applications of the single-electron transistor have been in memory, but some research has been directed towards building logic elements [1-

14][1-15]. The application of SETs to logic circuits is actually quite difficult, because these devices are quite sensitive to any spurious movement of charge in close vicinity. A fluctuation of the state of a charge trap or an impurity close to the SET can cause the logic element to generate a erroneous signal in the circuit. Thus, the most obvious application of the SET is in charge detection, rather than logic circuits.

Chapter 2 Fabrication

2.1 Lithography

As described previously, for single-electron transistors to be useful at temperatures easily attained with modern refrigeration techniques (T=50-300mK), the critical dimensions of these devices must be less than 100nm. Conventional photolithography does not allow faithful reproduction of patterns at such small dimensions. The impeding parameter of this technology is the relatively large wavelength of the radiation used to expose the resist (λ=365nm in most systems available at MIT, λ=248nm in modern photolithography systems used in industry today). When the wavelength of the radiation becomes comparable to the critical dimensions of the pattern, diffraction causes degradation of the pattern fidelity. So generally, the radiation wavelength should be much smaller than the pattern dimensions. The semiconductor industry has been able to use complex and expensive techniques such as phase shift masks [2-1] and optical proximity correction [2-2] to compensate for some of the diffraction effects and use radiation wavelengths (λ=248nm) that are comparable to the feature sizes (l=0.25μm). Even these techniques are not suitable for our needs, since they do not permit fabrication of features less than 100nm. Nevertheless, there are several other suitable lithography techniques. The two most matured nanolithography technologies to date are electron-beam lithography and x-ray lithography.

There are advantages and disadvantages to both x-ray and electron-beam lithography and there exist many arguments for using one versus the other. With the use of x-ray lithography ($\lambda \cong 1nm$), it is possible to pattern features on the order of 10-20nm. On the other hand, electron-beam lithography can be used to reproducibly make features of about 60nm on a substrate. The benefit of electron-beam lithography is that one can easily and quickly make modifications to a pattern without the need to make additional masks. This was a big advantage for us, so we chose electron-beam lithography for the fabrication of our devices.

We perform the lithography using the beam of a JEOL 6400 scanning-electron microscope (SEM) for transferring the pattern to a resist layer applied to our samples. For pattern generation, we use the Nanometer Pattern Generation System (NPGS) available from Joe Nabity Lithography Systems in Bozeman, MT. This system uses a PC with a digital to analog converter card to generate two linear voltage signals. These two voltage signals are fed to the input amplifiers of the X and Y scan coils of the SEM. So we are able to precisely control the position of the beam with the PC supplying the control signals. In addition, we use a third voltage signal from the PC to control the beam blanking circuit of the SEM to turn the beam off and on as desired.

The pattern is exposed on a point by point basis. Each pattern element written by our system is broken down into "simple" elements, such as boxes, circles and lines. Every element is filled in by scanning the electron beam across its entire area. Usually, the beam is scanned in a serpentine fashion to fill the area of each element. The beam scan is

performed by stopping at points spaced apart by a predetermined distance, unblanked for a time period to give every point the proper electron dose, blanked, and then moved on to the next point. Lines of minimal width are written with a single pass of the beam. We were able to obtain features with a minimum linewidth of 60-70nm.

The minimum point to point spacing of the digital-to-analog converter of the computer system is nominally 1.4nm with the field size of 90μm×90μm. The beam diameter of the microscope is about 10nm. This does not mean that we are able to write 10nm wide lines. There are numerous factors that degrade the ultimate pattern resolution of the lithography system. For example, focus drift limits the writing time to less than a few minutes, beyond which the surface of the substrate is no longer in the plane of optimal focus.

The most important factor in electron-beam lithography that limits the pattern linewidth is electron backscattering. As the electrons of the microscope beam impact the surface of the substrate, they scatter backwards into the resist. This effect increases the effective area of exposure in the resist, thus increasing the minimum attainable feature size. Besides obtaining the minimum possible critical dimensions, we need to have a large undercut in our resist profile, as will be discussed in the following sections. The backscattering process actually helps to increase to amount of undercut. Our solution to this dilemma is to optimize lithography parameters for minimum linewidth, including

minimizing the level of backscattering, and to obtain the necessary amount of undercut through other methods, which will be described later in this chapter.

The amount of backscattering generally decreases at higher accelerating voltages, so we use the highest voltage available on our electron-beam machine, 40kV. The level of electron backscattering also depends on the substrate material. We fabricated single-electron transistors on a variety of substrates: oxide coated silicon and GaAs wafers. Since the atomic weight of GaAs is higher than silicon, the lithography parameters for fabrication of our devices on these two substrates are different. We used oxide coated silicon wafers for the development of the general methods for the fabrication of single-electron transistors. On the other hand, all the SET charge-sensing experiments were performed on GaAs heterostructures with a two dimensional electron gas under the surface. This technique allowed us a great deal of flexibility in the type of structures that we used for our experiments. The exact parameters of the complete fabrication process are given in Appendix A.

2.2 Double-angle evaporation

The structure of our single-electron transistor consists of a small metal island coupled to the source and drain electrodes through two metal-insulator-metal (MIM) tunnel junctions. These tunnel junctions are essentially overlaps of two layers of metal with a thin dielectric layer in between. The dielectric has to be thin to allow electrons to tunnel

through. The tunneling rate defines the resistance of the tunnel junctions, and is exponentially dependent on the thickness of the dielectric. Since the tunnel-junction resistance is a very important parameter in the operation of our devices, we need to have precise control over the dielectric barrier thickness.

We chose to use aluminum for the fabrication of our devices because it readily forms a smooth, uniform surface oxide layer upon exposure to oxygen gas. The aluminum oxide layer serves as the dielectric tunnel barrier. There are other metals that can be used to form the dielectric tunnel barrier, such as Cr [2-3], but the oxidation of these materials is much more difficult than aluminum. For example, the formation of a tunnel barrier in a Cr-Cr_2O_3-Cr single-electron transistor takes about 15 hours in an atmosphere of pure O_2 [2-4].

Our device structure requires two layers of metal. Traditional planar techniques form multilayer structures in separate lithographic steps. In our case, the bottom metal layer would be patterned, and then a second lithography would be performed and a second metal layer would be deposited. The dielectric film would be created somewhere in between. Unfortunately, this method is not applicable to our process, because if the first aluminum layer is introduced into the atmosphere after deposition, it is immediately coated with a thick Al_2O_3 layer which is impossible to control precisely. So, as in the original work of Fulton and Dolan [2-5], we use the double-angle evaporation technique to fabricate the tunnel junctions. This method allows us to deposit the bottom metal layer, the dielectric layer and the top metal layer in a single vacuum cycle. The dielectric

tunnel barrier is deposited in vacuum under controlled conditions and then sealed with another metal layer on top. This way, we are able to accurately control the thickness of the dielectric layer and therefore the resistance of the tunnel junctions.

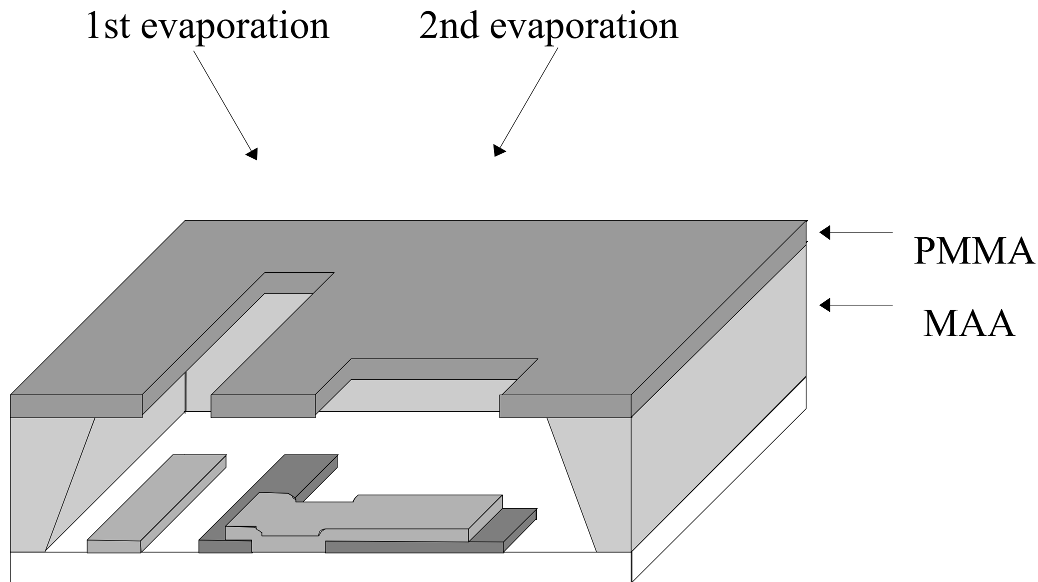


Figure 1. Double-angle evaporation.

The double-angle evaporation process is depicted in Figure 1. The aluminum layers are evaporated in an electron-beam evaporator, because its high degree of directionality gives us more control over the patterned metal. The sample is placed inside the evaporator on a tilting stage which can be rotated around an axis with the use of a vacuum feedthrough.

For the evaporation of the first layer, the sample is tilted at an angle of -10°. Then an aluminum layer 30nm thick is deposited at a rate of 0.5nm/second. This metal is shown in dark gray on the substrate surface in Figure 1. After a 10 minute cooldown period, the

high vacuum valve is closed and 50-100 mTorr of oxygen gas is introduced into the sample chamber. After the aluminum on the substrate is oxidized for 8-12 minutes, the oxygen is pumped out of the chamber. For the second aluminum evaporation, the sample stage is tilted at +10° to the normal. At this angle, an aluminum layer 350 angstroms thick is deposited. This metal is shown as light gray in Figure 1. As a result of the angled evaporations, an overlap is formed between the layers of metal formed in the first and second evaporations. This overlap area is the tunnel junction. Refer to the tunnel resistance data shown in Figure 7 for a 10 minute oxidation for an example of the dependence on the pressure of O_2 gas during oxidation. After the evaporations are completed, the sample is placed in acetone for "lift-off". The resist is dissolved in the acetone, leaving only the patterned metal on the substrate.

The double-angle evaporation technique allows us to fabricate tunnel junctions with a great degree of control and reproducibility. The only draw back to this method is that it inevitably results in undesired "shadow" features. In our experiments, we had to circumvent problems caused by these "shadow" features. One can imagine that in circuits requiring a high pattern density, the extra "shadows" could cause serious concern. Hence, the double-angle evaporation method is not applicable to a general fabrication process, rather it is best suited for specific applications, such as ours.

2.3 Resist profile

As a consequence of using a single lithography pattern to perform two evaporations at different angles, the pattern on the substrate surface occupies more area than the pattern on the surface of the resist. To allow for the extra room at the substrate surface, the double-angle evaporation requires a large degree of undercut in the resist profile. To achieve this, we use a bilayer resist structure, as shown in Figure 1. The bottom layer of the resist is a copolymer of poly-methyl-methacrylate (91.5%) and poly-methacrylic acid (8.5%), (PMMA, PMAA), which is 450nm thick. The top layer consists of 950,000 molecular weight poly-methyl-methacrylate (PMMA) which is 50nm thick. This layer serves to define the pattern of the evaporated metal on the substrate.

It is very important to be able to precisely control the degree of undercut in the resist profile. If the undercut is too small, then the sidewalls of the resist may become coated with metal after the angled evaporations. If the undercut is too large, then it is impossible to place two long parallel lines close together, because the resist in the top layer separating the two lines can fall without support in the bottom layer. We found several methods by which we are able to precisely control the undercut in the lower resist layer.

The most dependable method of controlling the resist undercut is UV flood exposure of the bottom resist layer. Immediately after spinning and baking, the bottom resist layer is uniformly exposed with 220nm UV radiation at a power density of $1mW/cm^2$ for a controlled period of time. Afterwards, the top resist layer is applied. After exposure, the

pattern is developed in a 2:3 solution of methyl-isobutyl ketone (MIBK) : isopropyl alcohol (IPA). The samples are then immediately rinsed in IPA for 30 seconds.

By using UV radiation to flood the bottom resist layer, we can precisely control the degree of undercut in the bottom layer. Figure 2 shows scanning-electron micrographs of line profiles for 0, 2, 3, and 4 minutes of UV flood exposure. The undercut, measured as the linewidth in the bottom resist layer, varies from 100nm for no UV exposure of the bottom resist layer to 550nm for a 4 minute UV exposure. We selected the process parameters corresponding to an undercut of 350nm, achieved with a 3 minute exposure.

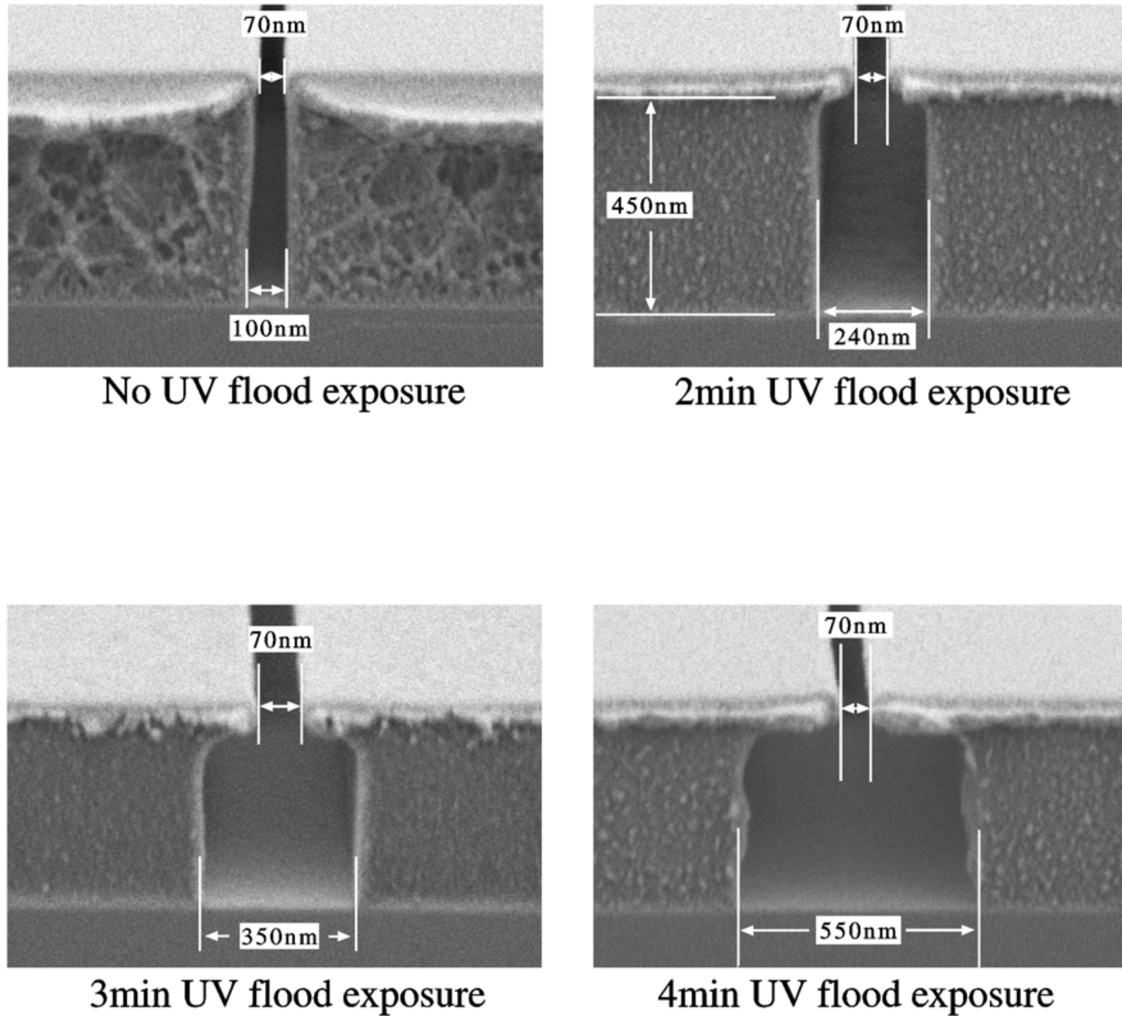


Figure 2. Effect of varying the UV exposure of the bottom resist layer on the cross-sectional profile. A 3 minute UV flood exposure is used in the SET fabrication process.

In addition to using UV flooding of the bottom resist layer to increase the undercut profile, we investigated several other methods. Among other techniques, we experimented with using two subsequent developing steps. After exposure, the samples are developed in the MIBK solution for 30 seconds. Then, the pattern is further developed in a 1:4 solution of poly-glycol methyl ether acetate (PGMEA) : ethyl alcohol for 30 seconds. The samples are then placed in isopropyl alcohol for 30 seconds. The

reason behind this procedure is that in the second development step, the PGMEA-based developer only dissolves the bottom MAA copolymer layer, leaving the top PMMA layer intact. Figure 3 shows the effect of using this two step development procedure on the pattern profile. The resist structure shown in Figure 3 is different from our usual resist structure. The thickness of the lower MAA copolymer layer is only 200nm, rather than the usual 450nm, and the top PMMA resist layer is 50 thick, as before. The effect of the PGMEA development is very convincing: the undercut in the lower resist layer is increased by a factor of 2. The increase of the linewidth in the top resist layer from 70nm to 100nm is due to resist damage in the SEM during inspection.

Ultimately, we used the UV flooding method for the fabrication of single-electron transistors. Our decision was based on some evidence of higher surface tension of the PGMEA-based developer. The high surface tension can cause damage to the thin top resist layer during the drying process. In fact, the high surface tension of the PGMEA-based developer caused some areas of the top resist layer to collapse, because as a consequence of the large undercut in the pattern profile, some areas of the top resist layer are not supported.

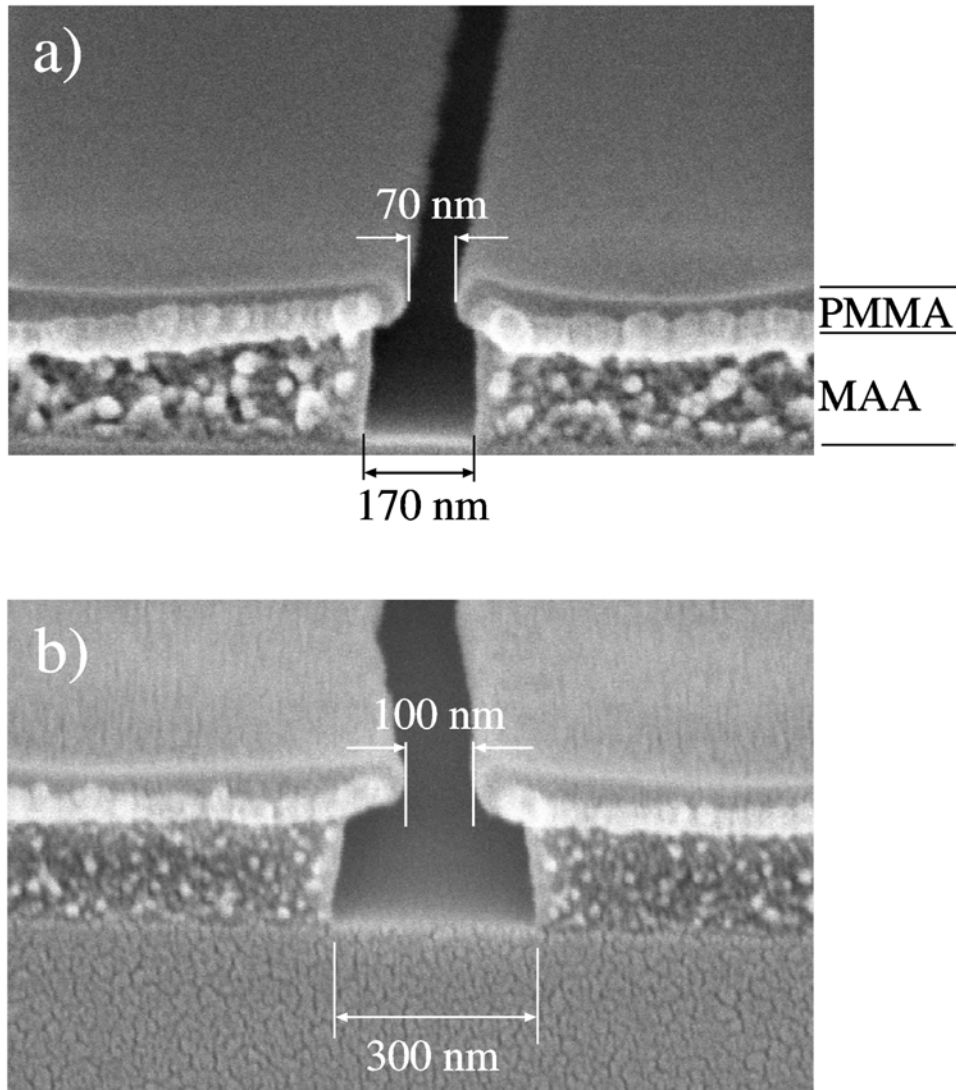


Figure 3. Effect of using a two-step development procedure. a) Profile of a single-pass line written in a bilayer resist. Development is performed in a 2:3 MIBK:IPA solution for 60s. b) The sample is developed in the MIBK solution for 30s and then further developed in a 1:4 PGMEA:ethanol solution for 30s. In both cases, the development process is completed by a 30s rinse in isopropanol.

The degree of undercut can be further increased by combining both techniques. By using both UV flooding of the bottom resist layer and the two-step development technique, it is possible to achieve an extreme degree of undercut in the pattern profile. Figure 4 shows a profile of a line that was fabricated by combining a 3 minute UV flood of the bottom MAA copolymer layer and the two-step development procedure.

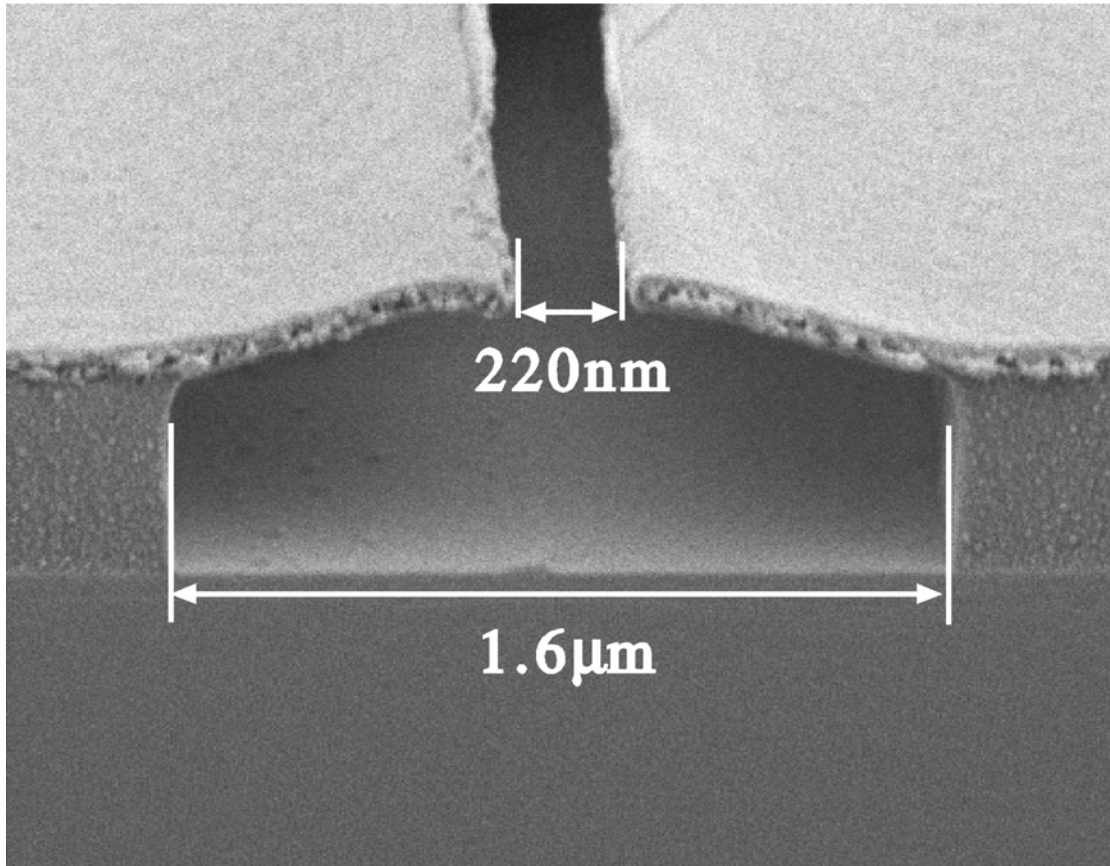


Figure 4. Profile of a single-pass line obtained with a 3 minute UV flooding of the bottom resist layer and the two-step development procedure.

Since the above described procedures are performed in order to obtain an optimal pattern profile to be used for double-angle evaporation, let's consider the effect of evaporating metal vapors on the surface of the organic polymer. Obviously, extreme heat can cause severe damage to the pattern. We have observed some evidence of resist flow under

extreme thermal conditions during some evaporations of nickel, a refractive metal, in a thermal evaporator.

We perform all our evaporations in an electron-beam evaporator, using a double-shutter system and a molten-metal source of limited area (~1cm^2). As a result, the effects of heating are minimal. Nevertheless, there is some degradation of the resist pattern due to metal evaporation. Figure 5 shows that the linewidth of the pattern decreases during evaporation, caused by the fact that the evaporated metal clusters do not stick immediately upon impact with the resist surface (i.e. less than 100% sticking probability), but scatter over a range of angles. As a result, an overhang is formed on the edges of the upper layer resist. This overhang increases with the thickness of the evaporated metal, limiting the aspect ratio of the evaporated metal to about one. Hence, the metal thickness is limited to less than the minimum linewidth.

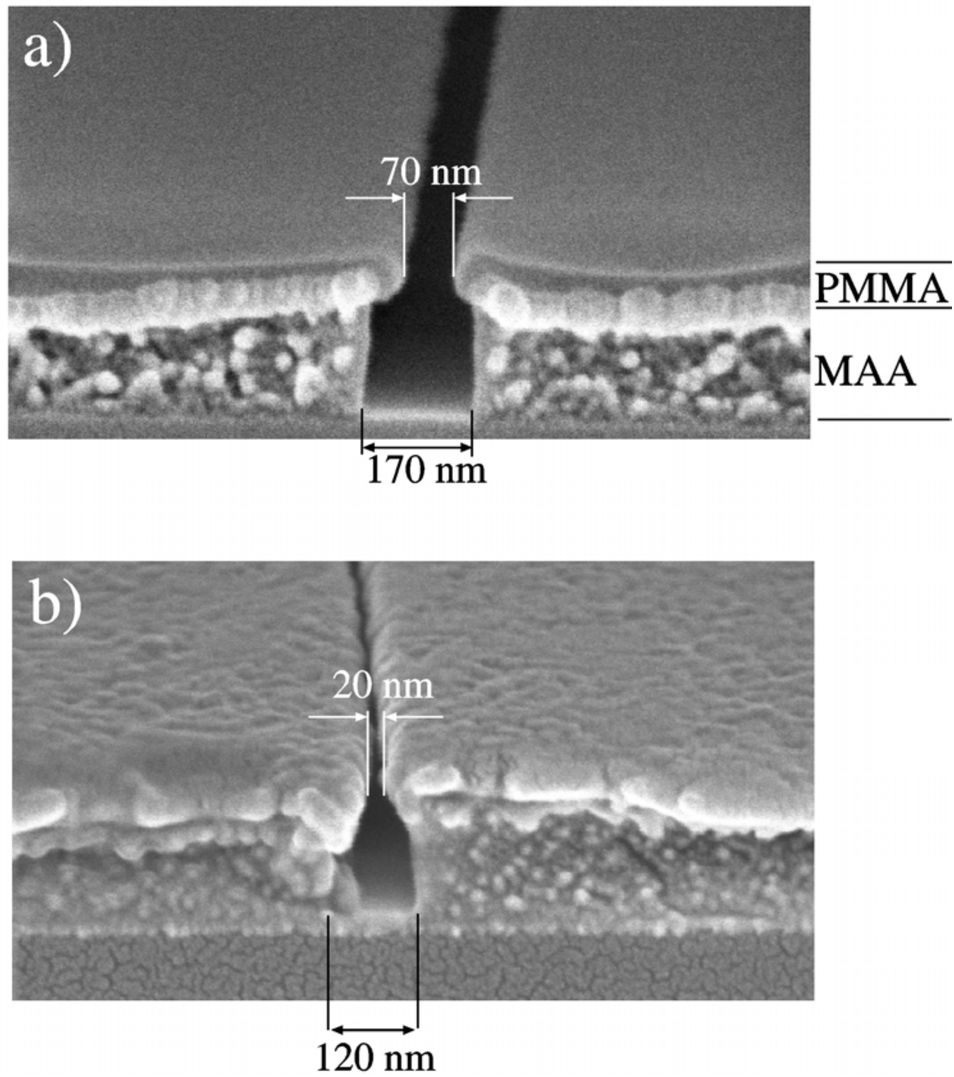


Figure 5. Effect of evaporating metal on the pattern profile. a) Profile of a single pass line in a bilayer resist. b) Profile of a single pass line after evaporating 50nm of aluminum.

2.4 Tunnel junction resistance

A tunnel junction made with the double-angle evaporation process described above is shown in Figure 6.

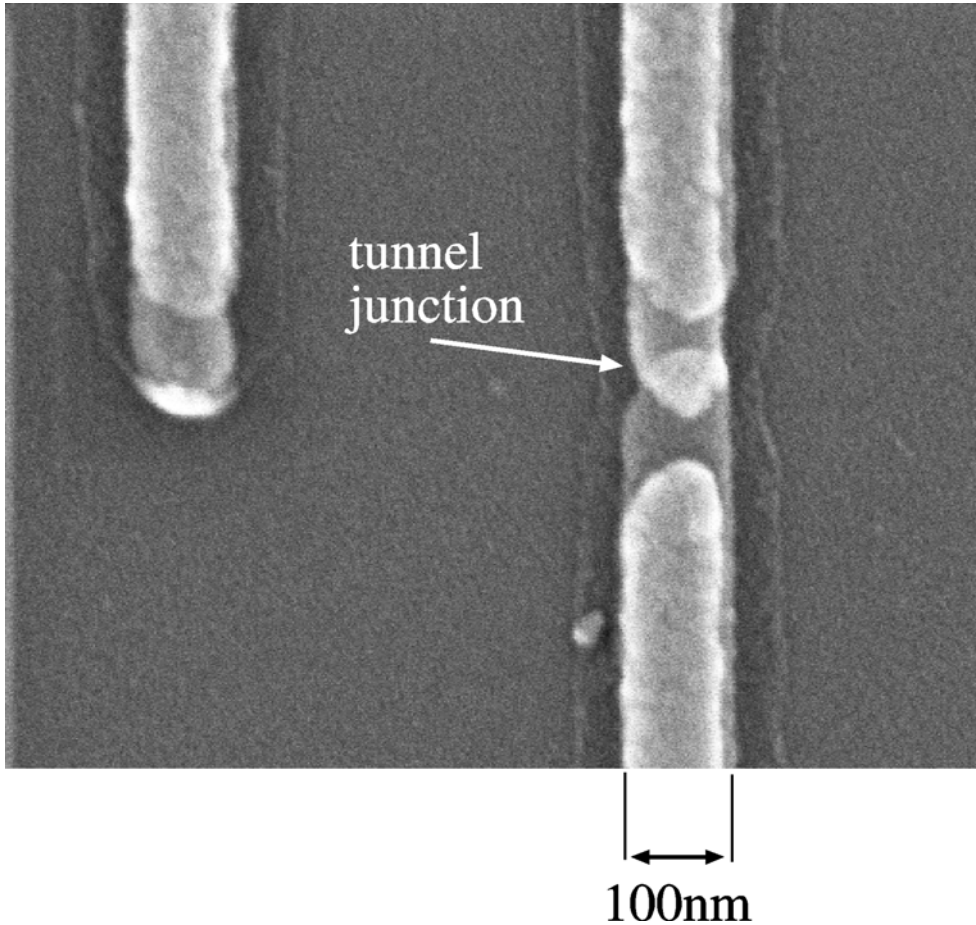


Figure 6. Scanning-electron micrograph of a tunnel junction made with the double-angle evaporation process.

This tunnel junction consists of an overlap of two layers of aluminum metal with a thin layer of dielectric (Al_2O_3) in between. The resistance of these tunnel junctions is very repeatable, because the oxidation is performed in a well-controlled environment. The dependence of the junction resistance on the oxygen pressure is best fit by a polynomial:

$$R = (2.8 \times 10^{-5}) P^3,$$

where R is the tunnel junction resistance in MΩ, and P is the oxygen pressure in mTorr. Figure 7 shows the tunnel junction resistances obtained for a 10 minute oxidation. The fact that the tunnel junction resistance has a power law dependence on the oxygen pressure, even though it is expected to have an exponential dependence on the barrier thickness could be explained by the fact that the barrier thickness does not grow linearly with the oxygen pressure.

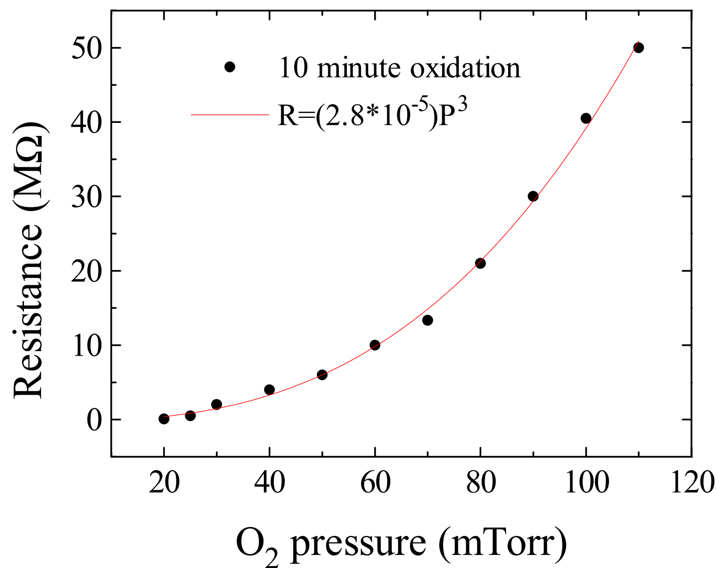


Figure 7. Dependence of the tunnel junction resistance on the oxygen pressure for a 10min oxidation. These results are for samples made on a Si/SiO_2 substrate.

These data were obtained for tunnel junctions fabricated on an oxidized silicon substrate. The resistance of tunnel junctions fabricated on a GaAs surface is much less reproducible, varying by as much as a factor of 2 for otherwise identical conditions. We

attributed this unpredictable variation to the surface morphology of the GaAs substrate. The oxidized silicon surface is very smooth, whereas the GaAs surface can be quite rough and variable from sample to sample. We have observed the surface of etched GaAs in a scanning-electron microscope, and measured the height variations to be as much as 10nm. Such a rough substrate surface could cause the dielectric of the tunnel barriers to grow irregularly. This would explain why on GaAs, the resistance of the tunnel junctions is more difficult to reproduce than on oxidized silicon.

Chapter 3 SET Operation

3.1 Coulomb blockade

The single-electron transistor (SET), as shown in Figure 8, consists of a small metallic island, referred to as the central island, coupled to source and drain electrodes through two small tunnel junctions. The SET is extremely sensitive to charge on its central island. A change of charge of a fraction of an electron in a near vicinity of the SET can cause significant changes in the current through the device. In fact, the current through the SET goes through periodic oscillations with additions of single electrons on the central island. The operation of the single-electron transistor is based on the principle of

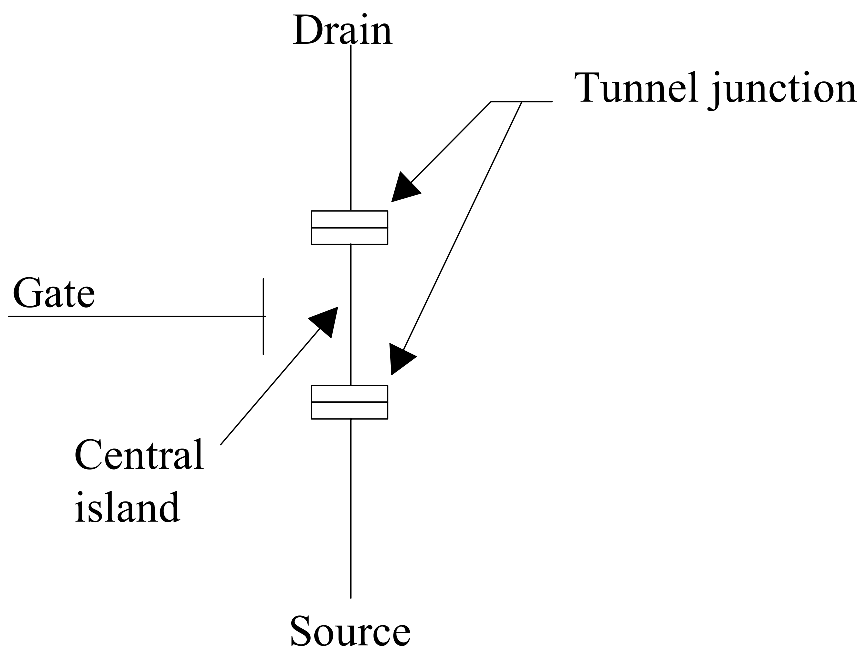


Figure 8. The Single-Electron Transistor.

Coulomb blockade [3-1][3-2][3-3][3-4]. The transfer of charge through the device is limited by a potential barrier determined by the electrostatics of the system. This electrostatic barrier arises from the discrete amount of energy it takes to increase the charge on a small metallic island by one electron.

For a description of the physics governing the operation of the SET, let us consider the source-drain current through the device in terms of the transfer of individual electrons. To traverse the device from source to drain, the electrons must tunnel onto the center island through one of the tunnel junctions and then tunnel off through the other. Thus, during this process, the charge on the central island must first increase by one electron, when an electron tunnels onto it, and then decrease to the original number of electrons when the electron tunnels off.

Since the central island is small, its capacitance to the environment, C_Σ, is small as well. Thus, the energy required to increase the charge on the capacitance of the central island by one electron, which is $E_c = e^2/2C_\Sigma$, can be quite significant. To travel from source to drain, the electrons must overcome this charging energy barrier.

If E_c is much larger than the thermal energy, $k_B T$, then electrons cannot be thermally excited over this energy barrier. Ideally, for a zero source-drain voltage bias, the current through the device is zero and the number of electrons on the central island is fixed. Of course, in a real situation, the current is a small but finite, mainly due to cotunneling events [3-5] [3-6] and finite temperature effects. In a cotunneling event, an electron

tunnels onto the island through one tunnel junction, and another electron tunnels off the island through the other tunnel junction. In effect, a charge of one electron is transferred across the transistor and the number of electrons on the central island remains unchanged. These cotunneling events are fairly rare and constitute a small addition to the source-drain current.

The above description holds true if the resistance, R_T, of both tunnel junctions satisfies the condition: $R_T >> R_Q$, where $R_Q = h/e^2 = 25.9k\Omega$ is the resistance quantum. In this case, the charge on the central island is well-defined. In other words, the level broadening due to increased coupling to the environment of states localized on the central island is smaller than the level spacing between the states. Otherwise, quantum fluctuations destroy the quantization of charge in Coulomb blockade, because the wavefunctions of the electrons would "leak" out into the leads, increasing the uncertainty in the location of the electrons. Later in this thesis, we describe an experiment that probes the physics of Coulomb blockade when the tunnel barrier resistances approach R_Q, and the degree of electron localization on the central island is substantially diminished.

The condition $E_c = e^2/2C_\Sigma >> k_B T$ is satisfied for low temperatures and a low central island capacitance. C_Σ is primarily determined by the capacitances of the tunnel junctions, which in a typical SET have areas of about $60\times60\text{nm}^2$, each with a capacitance of about 80aF (80×10^{-18} F). Typically, C_Σ is about 200aF, yielding a charging energy E_c of 0.4meV. A scanning-electron micrograph of an aluminum SET fabricated with the double-angle evaporation method is shown in Figure 9. This fabrication method is

described in Chapter 2. The maximum operating temperature for a SET with these parameters is about 1K.

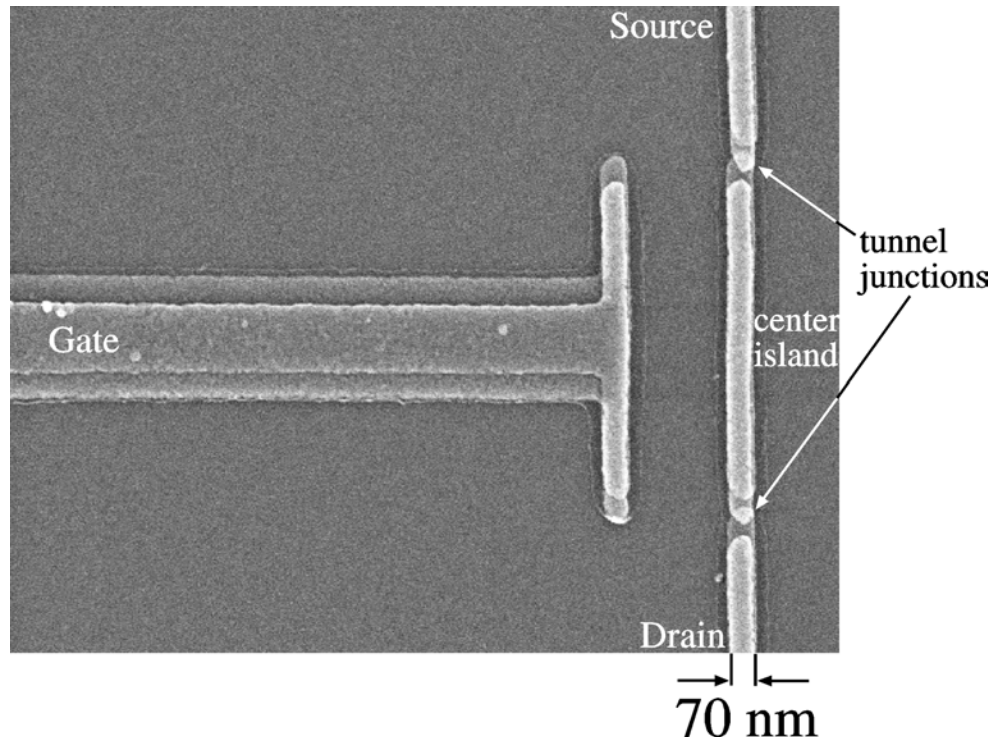


Figure 9. A scanning-electron micrograph of an aluminum SET fabricated with the double-angle evaporation method.

The electrostatic barrier to the transfer of electrons through the device can be varied with an external gate voltage. During the fabrication of the SET, we make a metal gate electrode in close proximity to the central island of the SET. This gate electrode has a certain gate capacitance, C_g, to the central island. A voltage applied to this gate electrode can raise and lower the height of the electrostatic barrier to the transfer of electrons through the device, resulting in a variation of the source-drain current. Actually, an SET can have several gate electrodes, all simultaneously affecting the current through the device, which can potentially lead to interesting applications.

By applying a voltage, Vg, to the gate electrode, we can induce charge on the gate capacitance to the central island, C_g, according to the expression: $Q_g = C_g V_g$. The electrostatic energy on the central island is a function of the number of electrons on the central island, n:

$$E_n = \frac{(Q_g - ne)^2}{2C_\Sigma}$$

Here, n is the integer number of electrons on the central island in excess of neutrality, and e is the charge of one electron. When $Q_g = (n + 0.5)e$, the electrostatic energies corresponding to n and n+1 are equal. At this exact point, the number of electrons on the SET central island can change between n and n+1 since the two states have an equal probability of occurrence. As a result, finite current can flow through the device at these points in gate voltage. As an electron tunnels onto the central island, the number of electrons on the central island shifts from n to n+1. Then, as the electron tunnels off the central island through the other tunnel junction, the number of electrons on the island shifts back to n. This process can be repeated indefinitely, resulting in a current through the device consisting of individual electron tunneling events. The total charge on the tunnel junctions, Q, is $Q = Q_g - ne$. When the number of electrons on the central island goes from n to n+1, Q is decreased by one electron.

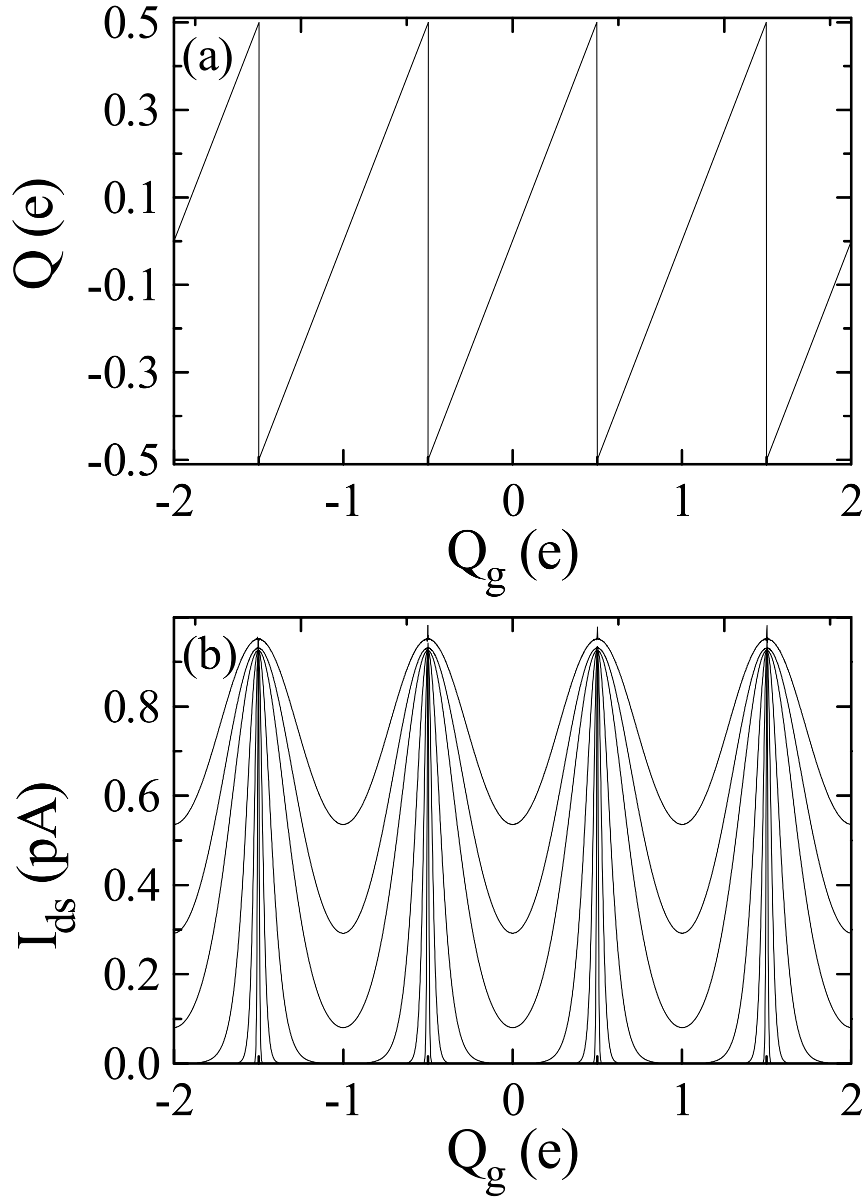
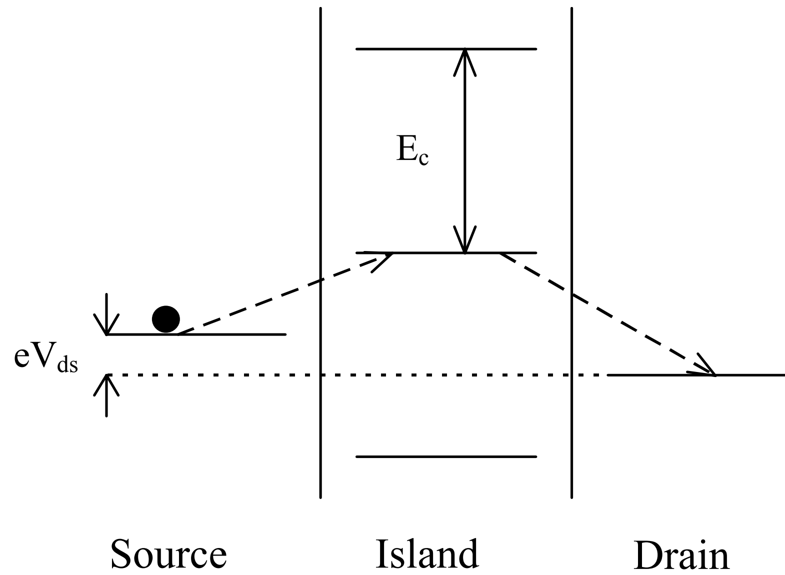


Figure 10. (a) The variation of the total charge on the tunnel junctions, Q, with the gate charge Q_g for zero temperature. At points where $Q_g=(n+0.5)$e, the number of electrons on the central island goes from n to $n+1$. (b) The source-drain current as a function of Q_g. The different curves correspond to temperatures of 0.02, 0.1, 0.3, 0.7, 1.0 and 1.3K.

Figure 10a shows the variation of Q with Q_g. Q varies linearly with Q_g, except at points where $Q_g=(n+0.5)e$. Here, the total charge on the tunnel junctions changes by $-e$ (where e is the absolute value of the electron charge), because the number of electrons on the central island shifts from n to $n+1$. At these points, the source-drain current displays a sharp peak, as shown in Figure 10b. In the case of zero temperature, the current through the device is nonzero only at points where $Q_g = (n + 0.5)e$. At higher temperatures, electrons can be excited on and off the central island at values of gate voltage in close proximity to these points, forming a peak. At even higher temperatures, these peaks broaden and eventually wash out. In our devices, this washing out occurs at temperatures of about 1-2K.



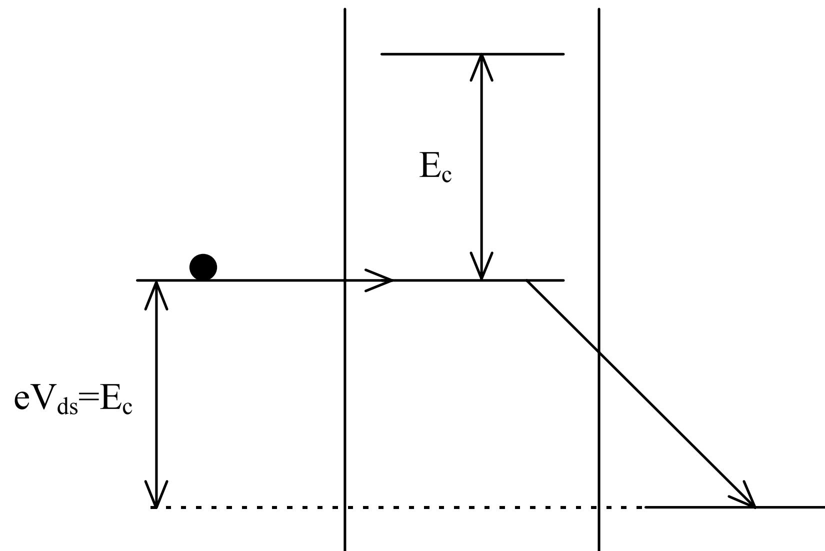


Figure 11. Energy diagrams of Coulomb blockade. a) Coulomb blockade condition - current is zero. b) The drain-source voltage bias is enough to overcome the charging energy barrier.

The Coulomb blockade principle can be further illustrated in the energy level diagrams in Figure 11. Figure 11a depicts the situation where the source-drain voltage bias, V_{ds}, is small and electrons cannot overcome the energy barrier, resulting in a zero current. Here, current flows through the device only when V_g is adjusted to align the energy levels

on the central island with the Fermi levels in the leads. Figure 11b shows the situation where $eV_{ds} = E_c$. This is the source-drain conduction threshold, given a "maximally blockaded" SET with $Q_g = ne$, where n is an integer. For larger V_{ds} biases, current through the device is only limited by the resistances of the tunnel junctions.

The manifestation of Coulomb blockade in the I_{ds}-V_{ds} characteristics of the single-electron transistor is a region of zero current for a range of small drain-source voltage biases. The maximum width of the Coulomb blockade region is equal to $2E_c/e$. Figure 12 shows an example of the I_{ds}-V_{ds} relationship of the SET for several values of gate voltage. Here, E_c is about 0.35meV. The width of the Coulomb Blockade is reduced from $2E_c/e$ to 0 as V_g is increased from 0 to 2mV. At this point, the charge induced on the central island by the gate is 0.5e.

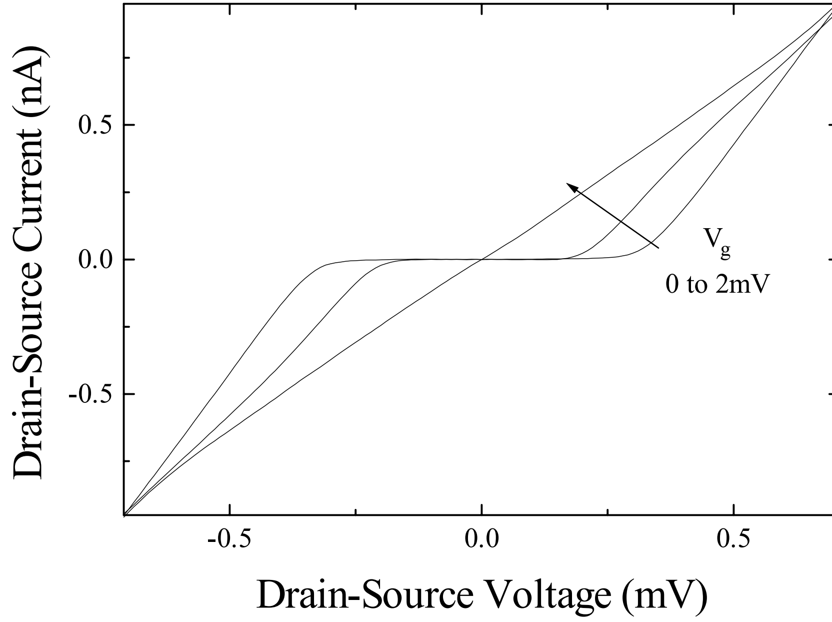


Figure 12. I_{ds}-V_{ds} of the SET at T=50mK. Vg=0, 1, 2 mV.

Since the single electron charging levels on the middle electrode are evenly spaced by E_c, the effect of gate voltage is periodic. The data shown in Figure 12 were obtained at a temperature of 50mK. At higher temperatures, the I_{ds}-V_{ds} characteristic becomes more rounded. We can detect no effects of Coulomb blockade for temperatures above 4K.

Figure 13 shows the dependence of I_{ds} on the gate voltage with increasing drain-source voltage bias. The current oscillates periodically with the period corresponding to an electron being added to the central island. This period corresponds to the gate voltage of: $P = \frac{e}{C_\Sigma}\frac{C_\Sigma}{C_g}$. The multiplier of $\frac{C_\Sigma}{C_g}$ is the lever arm necessary to convert the voltage applied to the gate electrode to the voltage that appears on the central island. The

amplitude of the oscillation depends on the drain source voltage bias. The largest amplitude occurs for $V_{ds} = E_c/e = 0.35\text{mV}$. This is consistent with Figure 12, where the largest change of I_{ds} with gate voltage occurs at a V_{ds} bias of 0.35mV.

We usually use the SET in small signal mode. This means that a small AC signal, V_{ac}, is applied to the gate of the device. The response of the SET current to this AC excitation can be expressed as: $I_{SET} = AV_{ac}$. Here, A is the gain, which is proportional to the slope of the I_{ds}-V_{gs} relationship, shown in Figure 13. Clearly, A is not a linear function of the DC gate voltage, V_g. The gain, A, of the SET can be Taylor expanded as: $A = \alpha V_g + \beta V_g^2 + \ldots$ The condition of linearity states that $\alpha V_g >> \beta V_g^2$. So, the amplitude of the AC signal, V_{ac}, must be maintained small, such that linearity holds at

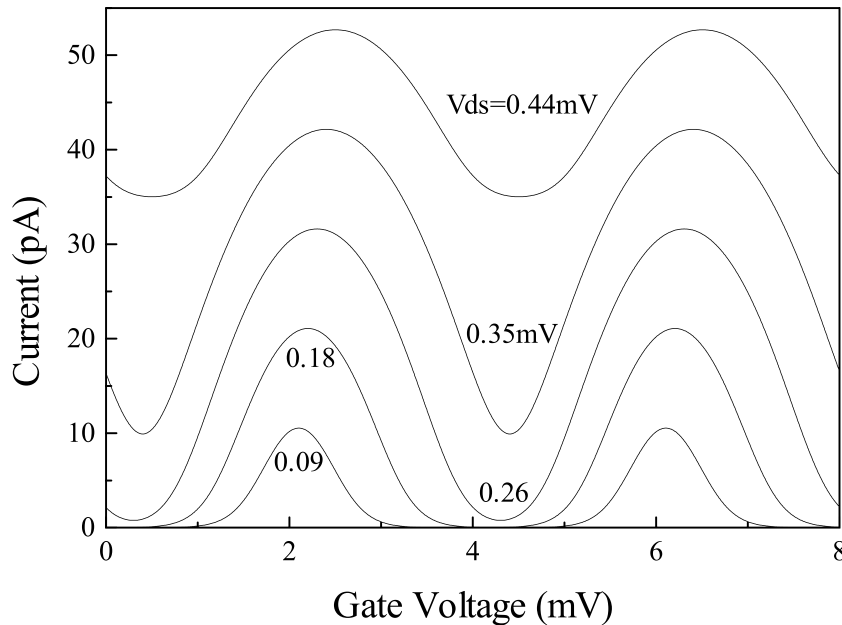


Figure 13. Dependence of the drain-source current on the gate voltage. The largest oscillation occurs for V_{ds}=0.35mV.

least in regions of high gain. The effect of gain and linearity of the SET amplifier in a charge measurement experiment will be shown in Chapter 5.

3.2 High frequency operation of a Single-Electron Transistor amplifier

Recently, there has been much research of electron levels in quantum dots. Some of the experiments with quantum dots involve capacitance spectroscopy, in which the quantum dot signal is capacitively coupled to an amplifier [3-7] that can detect single electrons tunneling on and off. Rather than studying quantum dots through tunnel conductance [3-8] [3-9], this type of measurement directly probes the charge on the quantum dot.

The SET has the highest charge sensitivity of any electronic device. But, a serious drawback is its high output impedance, which is normally above 100kΩ. If used by itself, the SET would be required to drive long coaxial cables from the sample space in the cryostat to room temperature electronics. These coaxial cables, which can be as long as 2-3 meters, present a large capacitance load (~1nF) to the output of the SET, and the response time of the output signal limits the measurement frequencies to less than a few kHz. There are two disadvantages to this situation. First, the noise level is significantly higher at low frequencies, so it is necessary to do a lot of signal averaging to obtain clean data. Second, low frequencies are unsuitable for experiments on phenomena that are susceptible to signal degradation due to leakage or decay.

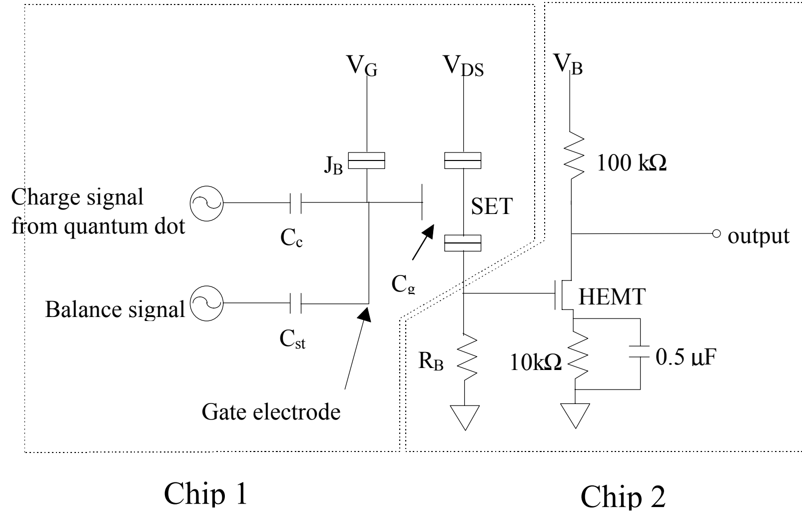


Figure 14. High frequency SET charge amplifier circuit.

We have combined the charge sensitivity of a SET with the frequency response of a High Electron Mobility Transistor (HEMT) amplifier to create a circuit that can push the cutoff frequency of a single SET amplifier out to 1MHz. A schematic of the circuit is shown in Figure 14. The entire amplifier consists of two chips. Chip 1 contains the SET and the device under study. In our experiments, usually this device is a quantum dot. Chip 2 contains the HEMT and the biasing resistors. Both chips are placed in the sample space in the cryostat and connections between the two chips are made with short 2-3mm bonding wires. This way, the capacitance load on the output of the SET is limited by the sum of the input capacitance of the HEMT transistor, the capacitance of the bias resistor, R_B, and the capacitance of the bonding wires. This technique reduces the capacitance load of the SET from about one nanofarad to a few picofarads.

The HEMT amplifier on Chip 2 is in the usual AC common-source configuration which provides for good gain and frequency characteristics. Since the source-drain voltage bias on the SET cannot be larger than a few millivolts, we use a 10kΩ resistor on the source of the HEMT to bias the DC gate-source voltage of the HEMT in a high gain regime. At frequencies higher than 300 Hz, the 10kΩ resistor is shorted out by the 0.5μF capacitor, essentially grounding the source of the HEMT in the AC regime. The resistor R_B is selected to match the resistance of the SET to optimize signal throughput. Its value is generally between 100kΩ and 1MΩ.

For high gain, the gate-source voltage bias of the HEMT has to be about -0.2V. Rather than grounding the source and applying a large negative voltage bias to the SET, we opted to use another biasing scheme. The voltage across the SET has to be small, on the order of 1mV, so for the purpose of the discussion of the HEMT bias, it can be thought of as grounded. The value of the HEMT drain bias voltage, V_B, is usually about 5V. We place a 10kΩ resistor on the HEMT source to raise its source voltage by about 0.2V. Under these conditions, the DC gate-source bias of the HEMT is about -0.2V. The 0.5μF capacitor that is connected in parallel to the 10kΩ resistor presents a low impedance path in AC mode, so the source of the HEMT is grounded for AC analysis.

The SET charge sensing stage is located on Chip 1. The gate electrode is capacitively coupled to the central island of the SET through a capacitance C_g and to the charge signal through a capacitance C_c. The capacitance of the gate electrode plays an important role in the performance of the SET amplifier.

In some charge sensing experiments, it is desirable to bias the voltage on the gate electrode. Since the gate electrode is used to sense time varying AC charge signals, the DC voltage bias has to be set through a resistive component. Unfortunately, typical thin-film meander line resistors have a large stray capacitance. Using such components would significantly reduce the charge signal that we are trying to measure. In the following discussion, we explain this phenomenon and propose a solution to this problem.

Lets denote the total capacitance of the gate electrode by C_{gt}. This capacitance can be expressed in terms of the circuit components in Figure 14 as: $C_{gt}=C_c+C_g+C_{st}+C'$. Here, C' denotes all the stray capacitance that adds to the total capacitance of the gate electrode. The capacitances C_c, C_g and C_{st} are all on the order of 40aF. Let us also denote the amplitude of the charge signal by Q_s. The fraction of Q_s that appears on the gate electrode is Q_sC_c/C_{gt}. The fraction of this charge that appears on the central island of the SET is further reduced by a factor of C_g/C_Σ, where C_Σ is the total capacitance of the SET central island. This means that the fraction of the charge signal that appears on the central island of the SET is equal to $Q_s(C_cC_g)/(C_{gt}C_\Sigma)$. If the stray capacitance, C', is large, the reduction factor $(C_cC_g)/(C_{gt}C_\Sigma)$ could be quite small. In order to keep this factor from completely destroying the signal, C' must be minimized. The largest contributor to C' is the capacitance of J_B, a tunnel junction that is used to bias the DC voltage on the gate electrode. Using a conventional bias resistor in the place of the bias tunnel junction would reduce the signal level greatly, because such resistors have stray capacitances on the order of picofarads. This means that the signal from the quantum dot

would be reduced by a factor of 10^6! The tunnel junction is our solution to this problem, because it has a capacitance of only about 80aF. With these values, the signal reduction factor $(C_c C_g)/(C_{gt} C_\Sigma)$ would be about 0.04, which is reasonable.

The resistance of junction J_B has to be about 10GΩ. Since the capacitance of the gate electrode is about 40aF, the charge leaks off the gate electrode at a characteristic RC decay time of 0.4μs. This means that charge detection must be performed at a rate faster than 0.4MHz. We have used the HEMT-based high frequency amplifier stage at frequencies up to about 1MHz, above which the stainless-steel coaxial cables of the cryoprobe start to attenuate the AC signal.

In order to eliminate the effect of distortion due to a background signal, it is possible to use a capacitance bridge technique. A standard capacitor is connected to the gate electrode, denoted as C_{st} in Figure 14. A balance signal is applied to this capacitor which is 90° out of phase with the charge signal. Since the C_{st} is a known value, which is approximately 40aF, it is possible to deduce the value of the capacitance under test by comparing the relative amplitudes of the in-phase and quadrature components of the AC signal response of the SET.

This charge detection scheme provides for high charge sensitivity at high frequencies. In contrast with experiments with SET electrometers with the central island directly coupled to the device being measured [3-10] [3-11], this scheme has two series capacitances to the central island, C_c and C_g. This way, the size of the SET Coulomb blockade region is

independent of the length of the gate wire and the size of the device being measured, which is a big advantage. Another advantage of this scheme is the ability to bias the gate electrode with a tunnel junction. This way, it is possible to always bias the SET in the high gain region, even if there is some time-dependent charge redistribution around the central island of the SET.

Figure 15 shows an example of the response of the SET charge amplifier circuit at a frequency of 500kHz. The source-drain voltage bias of the SET is swept, as a charge signal of 0.006*e* is applied to the gate electrode. The effective noise bandwidth of the measurements is $\mathrm{ENBW} = \frac{1}{4\tau}$, where τ is the lock-in time constant. So, for $\tau = 10\mathrm{ms}$, $\mathrm{ENBW} = 25\mathrm{Hz}$. The signal-to-noise ratio in Figure 15 is approximately 15, so the charge sensitivity of this measurement is $8 \times 10^{-5} \frac{e}{\sqrt{\mathrm{Hz}}}$. This measurement was performed in a ^{3}He cryostat with a base temperature of 300mK. The charge sensitivity that we demonstrated with this experiments is comparable to recently published results with active amplifiers next to the SET in the sample chamber of the cryostat [3-12] [3-13]. This high frequency charge sensitivity value is quite good, considering we obtained a charge sensitivity of $2 \times 10^{-4} \frac{e}{\sqrt{\mathrm{Hz}}}$ in an experiment without a high frequency output stage at a frequency of 10kHz and a temperature of 50mK. The temperature of the experiment affects the charge sensitivity greatly, since the Coulomb blockade region of the SET becomes severely rounded at temperatures approaching 1K. So, at 50 mK, the charge sensitivity of the high frequency setup could conceivably be as low as

$1 \times 10^{-5} \frac{e}{\sqrt{\text{Hz}}}$. This predicted sensitivity is comparable to the charge sensitivity in an SET-based circuit that uses no active components, but rather a tuned LC resonator that effectively increases the frequency of operation to about 1GHz [3-14].

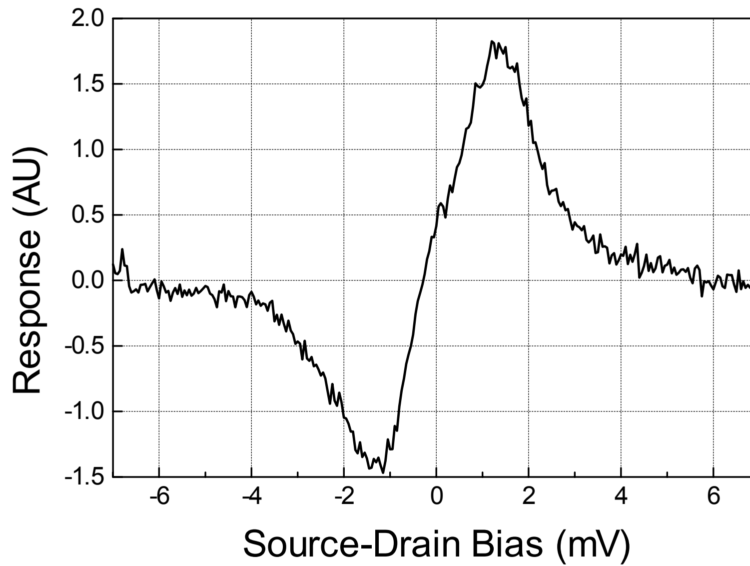


Figure 15. Output of the charge amplifier circuit at a frequency of 500kHz. T=300mK, AC amplitude on the gate=0.006 electrons, ENBW=25Hz.

3.3 Superconducting Single-Electron Transistor

Aluminum is a superconducting metal below a critical temperature of 1.18K [3-15] at zero magnetic field. Since we use the aluminum SETs in experiments below this temperature, we examined the behavior of these devices in the superconducting state.

The physics of the superconducting SET is rather complex and has been the subject of a great amount of research. The interaction of the Josephson energy of each tunnel junction, which is a measure of coupling of the superconducting wave function Ψ across the tunnel barrier, and the charging energy gives rise to many interesting phenomena. For example, experimentalists have observed one- and two-electron periodicity in the dependence of the current through the device on the gate voltage [3-16], and this dependence has also been shown to be sensitive to the presence of an even or odd number of electrons on the central island [3-17]. But, since the goal of our research has been to develop techniques for utilizing the SET as a charge sensor, rather than studying the physics of the superconducting SET, we were mainly interested in the effect of the superconducting properties of the SET on our charge measurement experiments.

The maximum voltage width of the zero current region of a superconducting SET is much larger than it is in the normal state. This width is $(4\Delta + E_c)/e$, where $\Delta = 0.18\text{meV}$ is the superconducting gap of aluminum [3-15], and E_c is the charging energy of the SET in the normal state. As with bulk aluminum metal, the superconducting properties of the aluminum SET are suppressed by applying a magnetic field through the sample. Figure 16 shows the dependence of the current-voltage characteristics of the single-electron transistor on the magnetic field penetrating the sample. This measurement was performed at a temperature of 50mK, well below the critical temperature of aluminum.

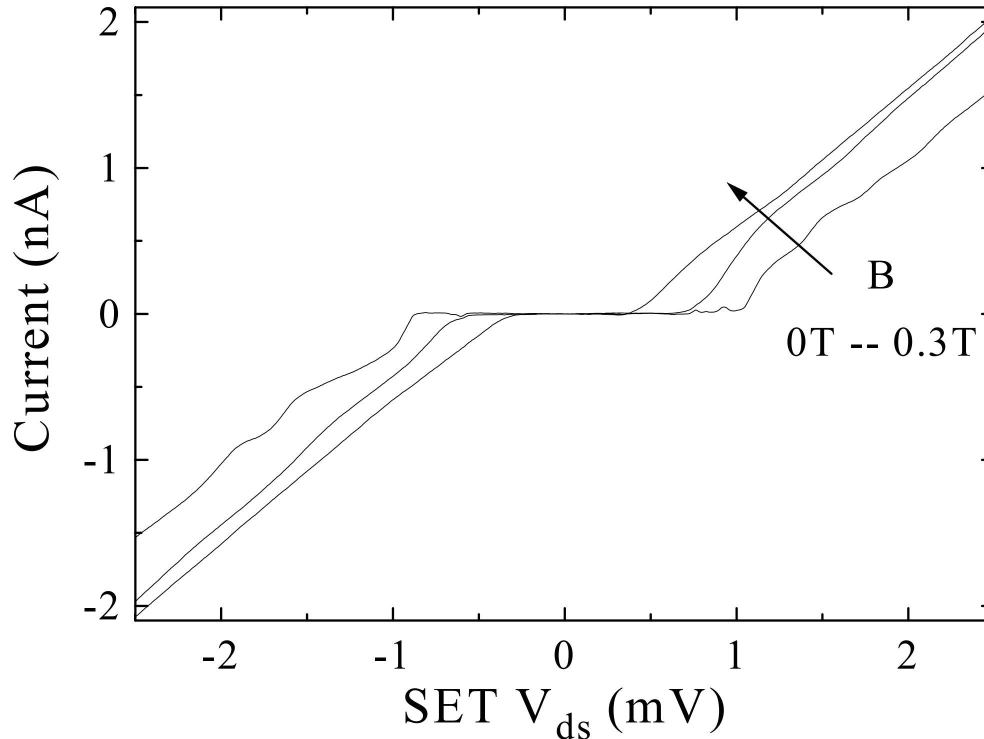


Figure 16. The dependence of the current-voltage characteristics of the SET on magnetic field. T=50mK. The magnetic field, B, is increased from 0T to 0.3T.

It is clear that the maximum voltage width of the zero current region decreases from about 1mV for a zero magnetic field to about 0.35mV, its value in the normal state for a magnetic field of 0.3T. Further increase of magnetic field has no effect on the characteristics of the SET. It is interesting to point out that even though the critical field of bulk aluminum is only 0.0105T [3-15], above which the superconducting properties of the material are suppressed, we need to apply a magnetic field as large as 0.3T to suppress the superconducting behavior of the aluminum SET. This can possibly be attributed to the fact that in the fabrication of the SET, we use thin films of aluminum, which could possibly have different superconducting properties than bulk material.

Nevertheless, the increased critical field does not affect the application of the SET to the charge sensing measurements greatly, since we use magnetic fields as high as 10-12T in our experiments on quantum dots.

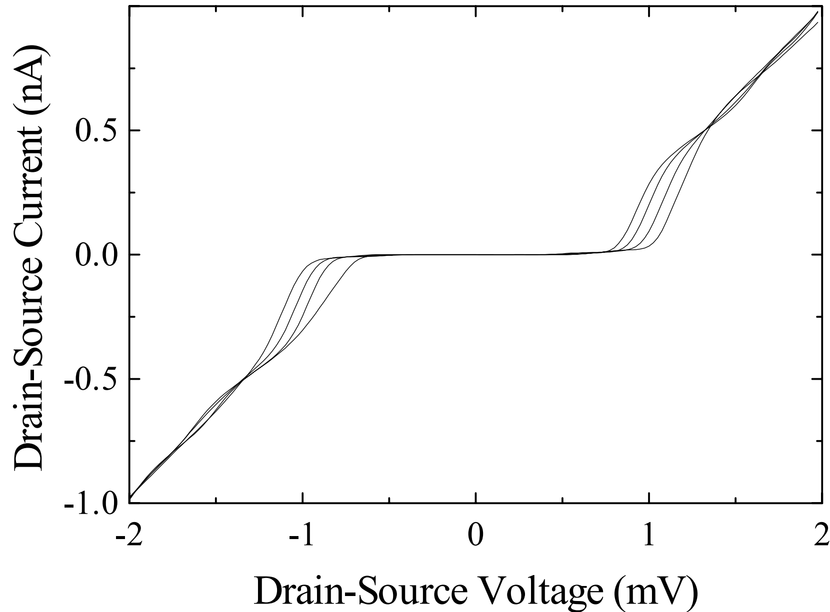


Figure 17. The dependence of the current-voltage characteristics of a superconducting aluminum SET on the gate voltage. T=50mK, B=0T, V_g is varied from 0 to 1mV.

Figure 17 shows the dependence of the current-voltage characteristics of a superconducting aluminum SET on the gate voltage. This measurement was also performed at a temperature of 50mK. In contrast with the SET in the normal state, a large portion of the zero-current region in the current-voltage characteristics of the SET remains virtually unchanged as the gate voltage is varied. It should be pointed out that the larger maximum voltage width of the zero current region and the sharp changes in the source-drain current at the onset of conduction ($V_{ds} \cong 1\text{mV}$) increases the charge

sensitivity of the SET in the superconducting state. We utilized the increased charge sensitivity of the superconducting SET in some charge sensing experiments.

Chapter 4 Floating Gate

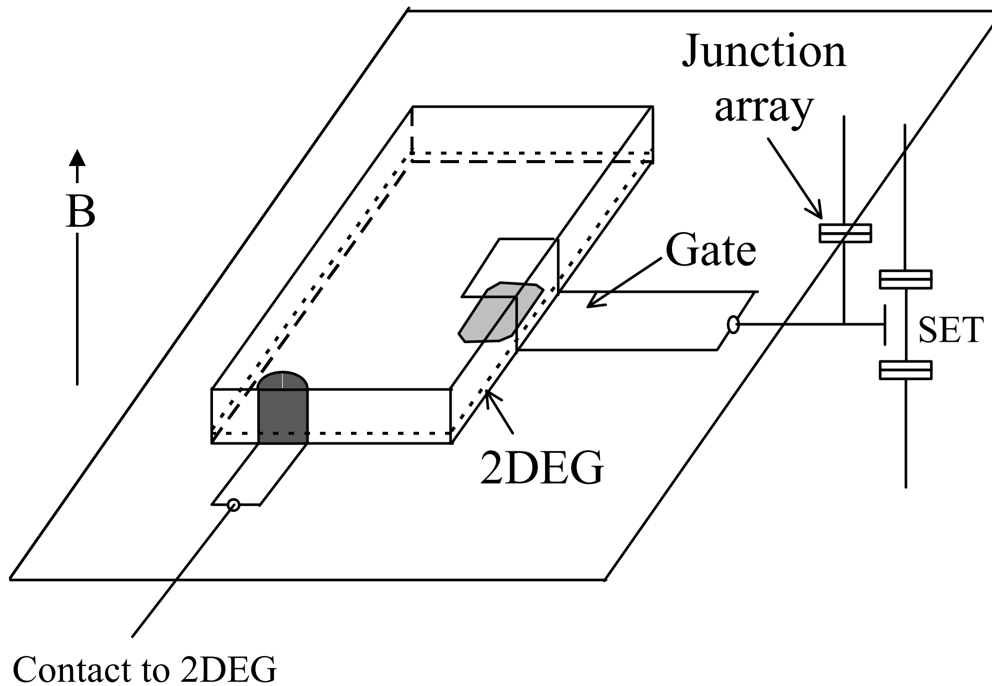


Figure 18. Schematic of the floating gate experiment.

We use a SET-based circuit to measure the chemical potential fluctuations of a two-dimensional electron gas (2DEG). The schematic of the experiment is shown in Figure 18. We use a GaAs/AlGaAs heterostructure with a 2DEG 100nm below the surface and etch a mesa to isolate the 2DEG to a section of the sample. Ohmic contacts allow metal leads to make good electrical contact to the 2DEG. We fabricate an SET to the side of the mesa, with an array of 5 tunnel junctions connecting to the gate electrode to permit DC voltage biasing on the gate electrode. The gate electrode capacitively couples to the central island of the SET and also extends over the top of the mesa a distance of about 1

micron. The gate electrode, thereby capacitively couples the SET to the 2DEG. The tunnel junction array would permit us to vary the electron concentration in the 2DEG directly under the gate lead. Unfortunately, we had a break in the wire connecting the junction array with the outside world. This prohibited application of a potential to the gate through the junction array. This essentially results in the gate electrode being connected to a floating charge reservoir through an array of 5 tunnel junctions.

4.1 Electron hopping

We apply a DC voltage to the 2DEG and a small (160μV, 17Hz) AC excitation. The source-drain voltage of the SET is biased to ensure optimal gain. The SET current is measured using a current lock-in amplifier that is referenced to the AC excitation signal. The experimental data shown in Figure 19 were obtained in two different cooldowns..

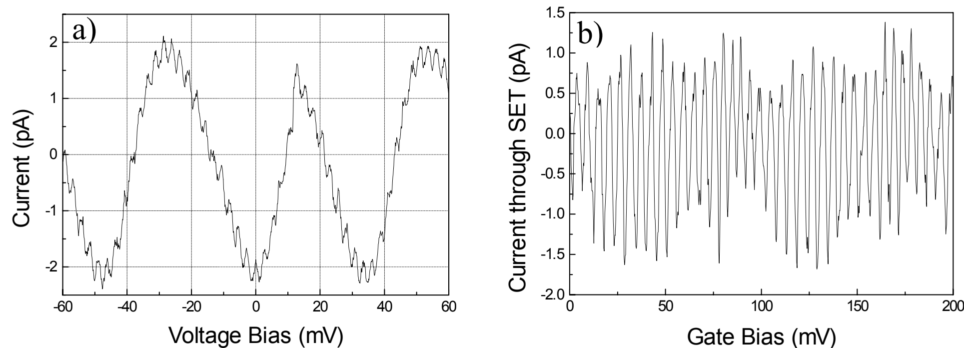


Figure 19. Response of the SET to variation in the DC potential of the 2DEG a) and b) are different cooldowns.

The measurements for each cooldown have very different characteristics. This arises because the 2DEG is coupled to the central island of the SET in two different ways.

First, the 50 mV periodicity in Figure 19a, is caused by capacitance coupling the 2DEG directly to the central island of the SET. This capacitance gives rise to a periodicity of about 75 mV in Figure 19b. This feature will be explained further below. Second, the 2DEG is capacitively coupled to the array of tunnel junctions, which is in turn capacitively coupled to the SET central island. When the DC potential of the 2DEG is varied, capacitive coupling to the array causes electrons to hop from island to island in the array. The SET senses this electron hopping, and we believe this is the origin of the signal that we observe with the periodicity of 3 mV which is present in both Figure 19a and Figure 19b.

The fact that the amplitude of the electron hopping signal is much bigger in Figure 19b than in Figure 19a can be explained by the fact that the electron concentration in the 2DEG can vary quite substantially between different cooldowns if the potential on the surface gate is not held fixed. In the case of Figure 19b, the 2DEG is fully depleted under the gate. In this caes, the capacitance between the gate electrode and the 2DEG is very small. Indeed, the capacitance between the gate electrode and the central island of the SET represents a major fraction of the total capacitance of the gate electrode. This means that most of the signal caused by electron hopping in the tunnel junction array appears at the central island of the SET, and the resulting current signal is quite large.

4.2 Magnetic field dependence

We have measured the variation of the chemical potential in the 2DEG with the magnetic field. We applied a magnetic field perpendicular to the 2DEG and measured the AC current through the SET, while keeping all the DC biases constant. The changes in chemical potential in the 2DEG cause the charge on the floating gate to shift. This occurs because the floating gate is capacitively coupled to the 2DEG. Since the SET is sensitive to any variations of charge in the proximity of the central island, the current through the device reflects any changes in the chemical potential. The data from this experiment are shown in Figure 20.

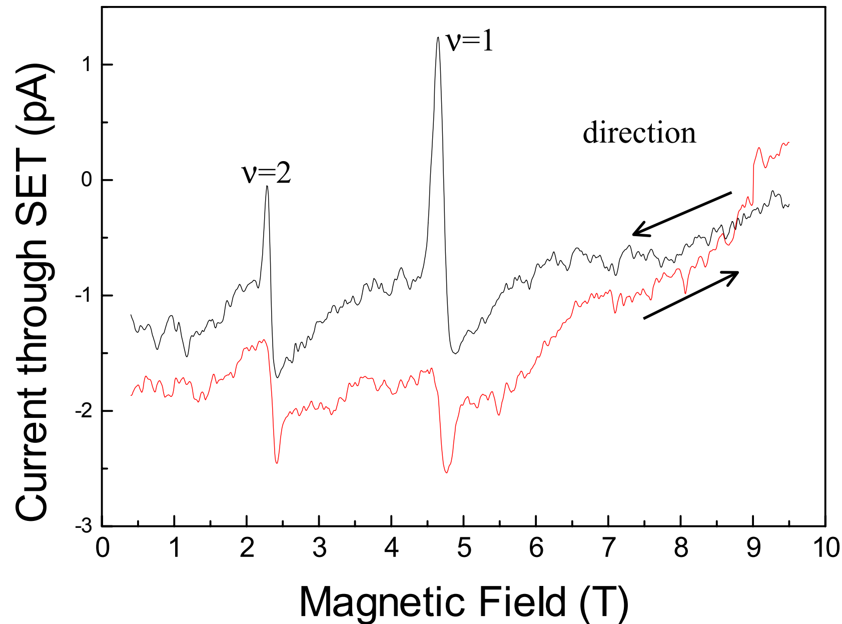


Figure 20. Sweep of magnetic field perpendicular to the 2DEG. B is swept at a rate of 1T/min.

Large features occur at points in the magnetic field that correspond to integer filling factors in the 2DEG. The 2DEG Fermi level changes abruptly when the magnetic field is swept through these values, and this leads to changes in the charge under the gate. This effect is very similar to previous results of floating gate measurements on samples 10,000,000 times larger in size [4-1]. The sharp peaks arise from eddy currents set-up in the 2DEG by the changing magnetic field. The direction of magnetic field sweep affects the sign of these peaks. Data taken by sweeping the magnetic field at much slower rates do not display the peaks. Rather, the SET output reflects the abrupt transition of the Fermi level as each successive Landau level depopulates. This observation has also been made elsewhere. [4-2]

Chapter 5 Quantum Fluctuations

5.1 Introduction

In classical physics, a puddle of electrons holds a discrete and measurable number of electrons. Quantum mechanics instead dictates that the probability for an electron to be in a localized state on the puddle depends on the coupling strength to the environment. For many systems in which a single state is coupled to a continuum, this coupling produces a "lifetime broadening" of energy levels. The Heisenberg Uncertainty Principle

$$\Delta E \Delta \tau \geq \hbar$$

states that it is impossible to have precise information both about the energy, E, of a particle and the time, τ, that the particle spends at that energy. As the coupling between a localized state to the environment increases, the lifetime of a particle on the state shortens. As a result, the uncertainty in the energy level increases. The precise shape of the broadened energy distribution depends on the system and the type of coupling.

Atomic spectra display a characteristic Lorentzian lineshape broadening [5-1]. In analogy with atomic spectroscopy, several experiments have demonstrated the capability of precisely measuring the energies to add electrons to quantum dots [5-2][5-3][5-4]. In contrast to atomic physics, the lineshape of quantum dot levels originates essentially in a many-body interaction between electrons in the dot and the macroscopic environment.

As in the previous discussion of single-electron transistors, the physics of quantum dots is primarily determined by Coulomb blockade in the many-electron regime. As the tunnel barrier conductance, G, between the quantum dot and the macroscopic leads is increased above $\frac{2e^2}{h}$, charge in the dot is no longer quantized and the Coulomb blockade is destroyed. This process has been attributed to quantum charge fluctuations between the dot and the environment [5-5]. A thorough physical description of this effect has only been recently proposed in the nearly closed regime $G << \frac{e^2}{h}$ [5-6][5-7] and the nearly open regime $\frac{2e^2}{h} - G << \frac{e^2}{h}$ [5-8].

Experiments measuring the charge or the capacitance of a dot provide the most direct information about charge fluctuations and the effect of the dot-environment interaction on the charge states of the dot. However, transport measurements have been the first to address the issue of dot-environment coupling. In one of the first studies, Foxman et. al. [5-9] examined the lineshape of conductance peaks with increasing coupling of the dot to the leads and found good agreement with Lorentzian broadening. To analyze the charging lineshapes in the dot for a broad range of coupling strengths, conductance measurements are poorly suited, being complicated by other processes such as cotunneling [5-10] and Kondo coupling [5-11].

Previous experiments have addressed the issue of charging lineshapes. Experimenters employed a semiconductor electrometer [5-12] to observe the effect of charge

fluctuations. They modeled their results by a reduction of the charging energy with increasing coupling. In another experiment, the effect of tunnel barrier conductance on Coulomb blockade was studied through peak splitting of double dots [5-13]. In this case, the spacing between double-dot peaks can be predicted with a similar formalism as we use in our lineshape analysis [5-14].

We have developed an experiment which probes the capacitance lineshape of a quantum dot with unprecedented sensitivity. We find that the lineshapes deviate substantially from previously employed fitting forms [5-9][5-12] and are best described for all coupling strengths by the theory developed recently by Matveev [5-7][5-8]

5.2 Experimental setup

We measure the capacitance lineshapes of a quantum dot with only one contact to a charge reservoir. The quantum dot is electrostatically defined in a two-dimensional electron gas (2DEG) of a AlGaAs/GaAs heterostructure. The 2DEG is about 120nm below the surface with a carrier concentration of $1\times10^{11}\,\mathrm{cm}^{-2}$. Measurements were performed on six different samples, each yielding very similar results, and here we present detailed data from two of them. Figure 21 shows a micrograph of the structure. The estimated area, A, of the quantum dot is about $0.5\mu\mathrm{m}^2$, which corresponds to a single particle energy level spacing of $\varepsilon = \dfrac{1}{A\rho(E)} = \dfrac{1}{0.5\mu\mathrm{m}^2\left(\dfrac{2m^*}{2\pi\hbar^2}\right)} = 7\mu\mathrm{eV}$.

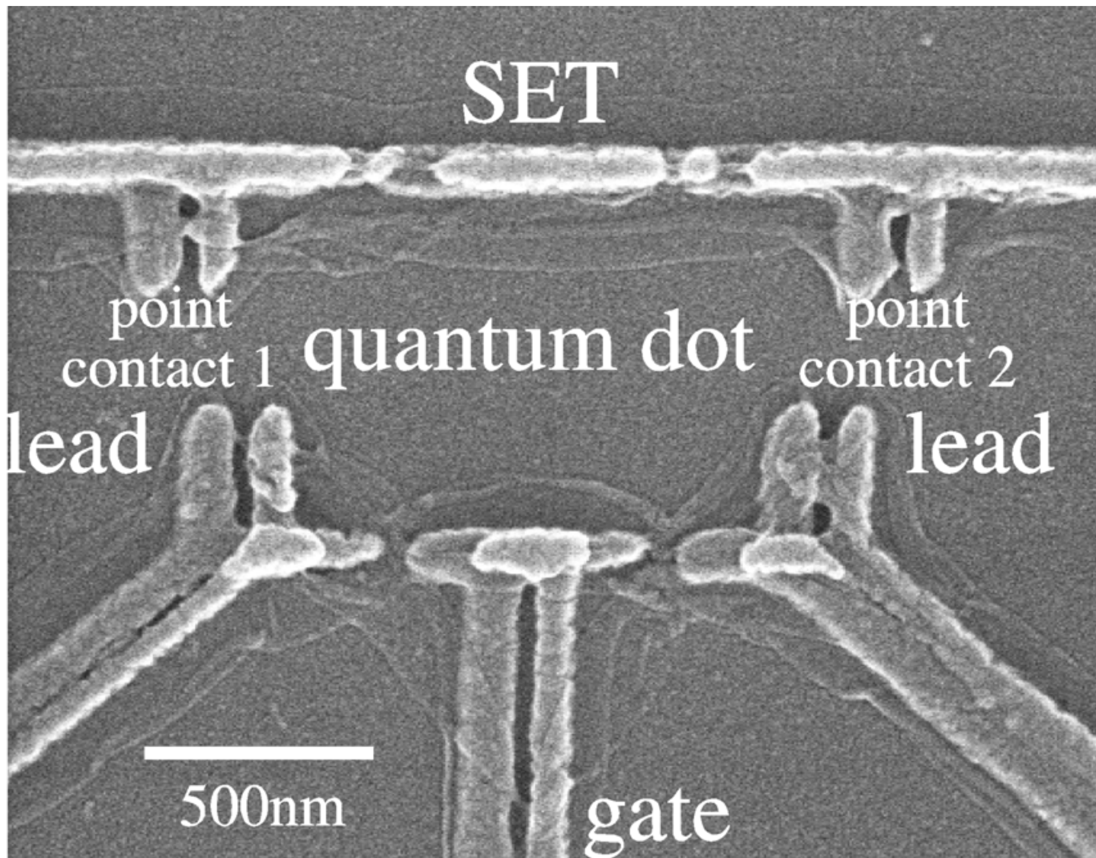


Figure 21. Micrograph of the measurement setup. The leads are made of aluminum by shadow evaporation. The area of the quantum dot is approximately 0.5μm^2.

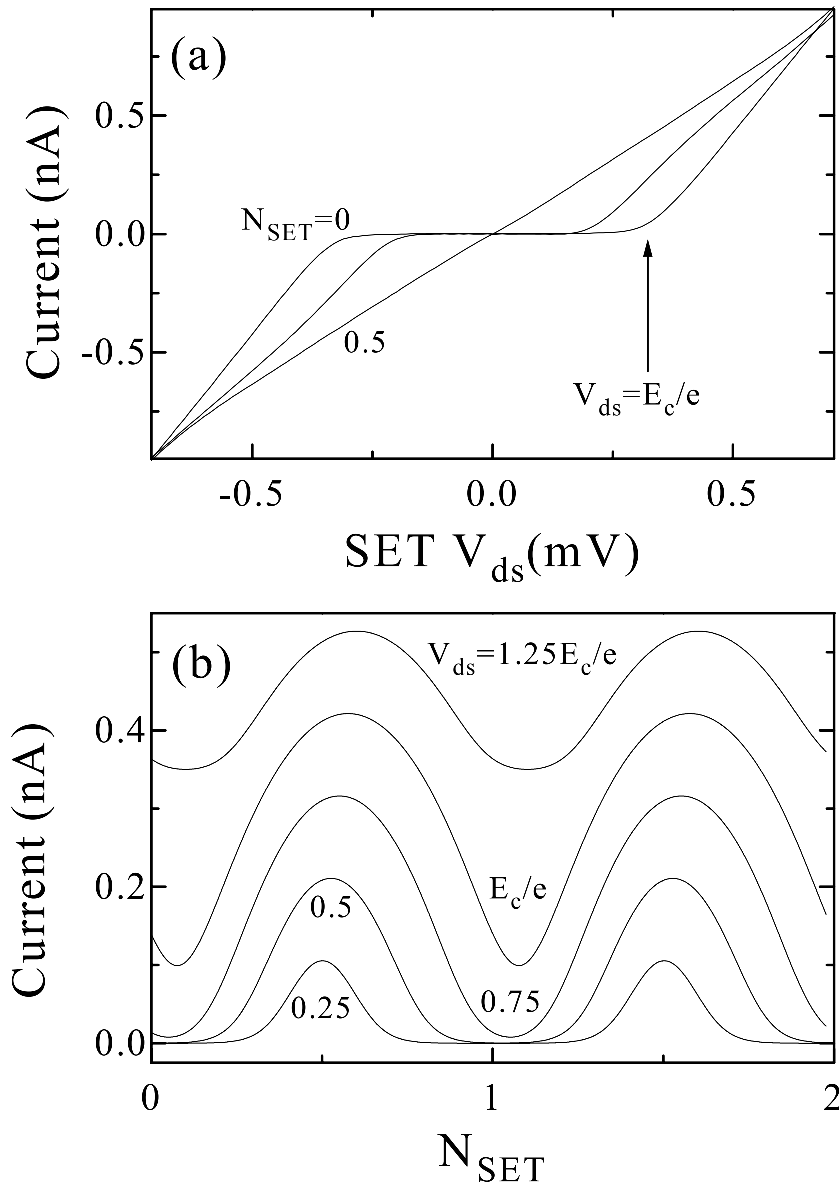


Figure 22. (a) Example of drain-source current-voltage characteristics of a single-electron transistor at a refrigerator temperature of 50mK shown for three values of gate voltage $C_{gs}V_g=eN_{SET}$=0, 0.25 and 0.5 electrons. The arrow shows the drain voltage bias for optimal gain. (b) Dependence on gate voltage of the SET current with transparent quantum dot tunnel barriers for 5 different drain-source voltage biases. Maximum peak-to valley modulation amplitude is at SET $V_{ds}=E_c/e$.

The charge on the quantum dot is measured with a single-electron transistor (SET) with extremely high sensitivity [5-15]. The metal SET is fabricated [5-16] with Al-Al_2O_3-Al tunnel junctions using the standard shadow-evaporation
method [5-17]. To maximize the sensitivity to the quantum dot charge, we incorporate the SET directly into one of the leads defining the dot.

Figure 22a shows the drain-source current-voltage relationship of the SET. It changes cyclically with the charge induced on the central island of the SET. The dependence of the current on the SET central island charge is shown in Figure 22b. For optimal charge sensitivity of the SET, we set the drain-source voltage at the onset of conduction for the maximum Coulomb blockade condition [5-18], as shown by the arrow in Figure 22a. For the sample primarily discussed in this chapter, we achieve a sensitivity of $1.2\times10^{-3}\frac{e}{\sqrt{Hz}}$ to the quantum dot charge, whereas the sensitivity of the SET to charge on the central island is $6\times10^{-5}\frac{e}{\sqrt{Hz}}$.

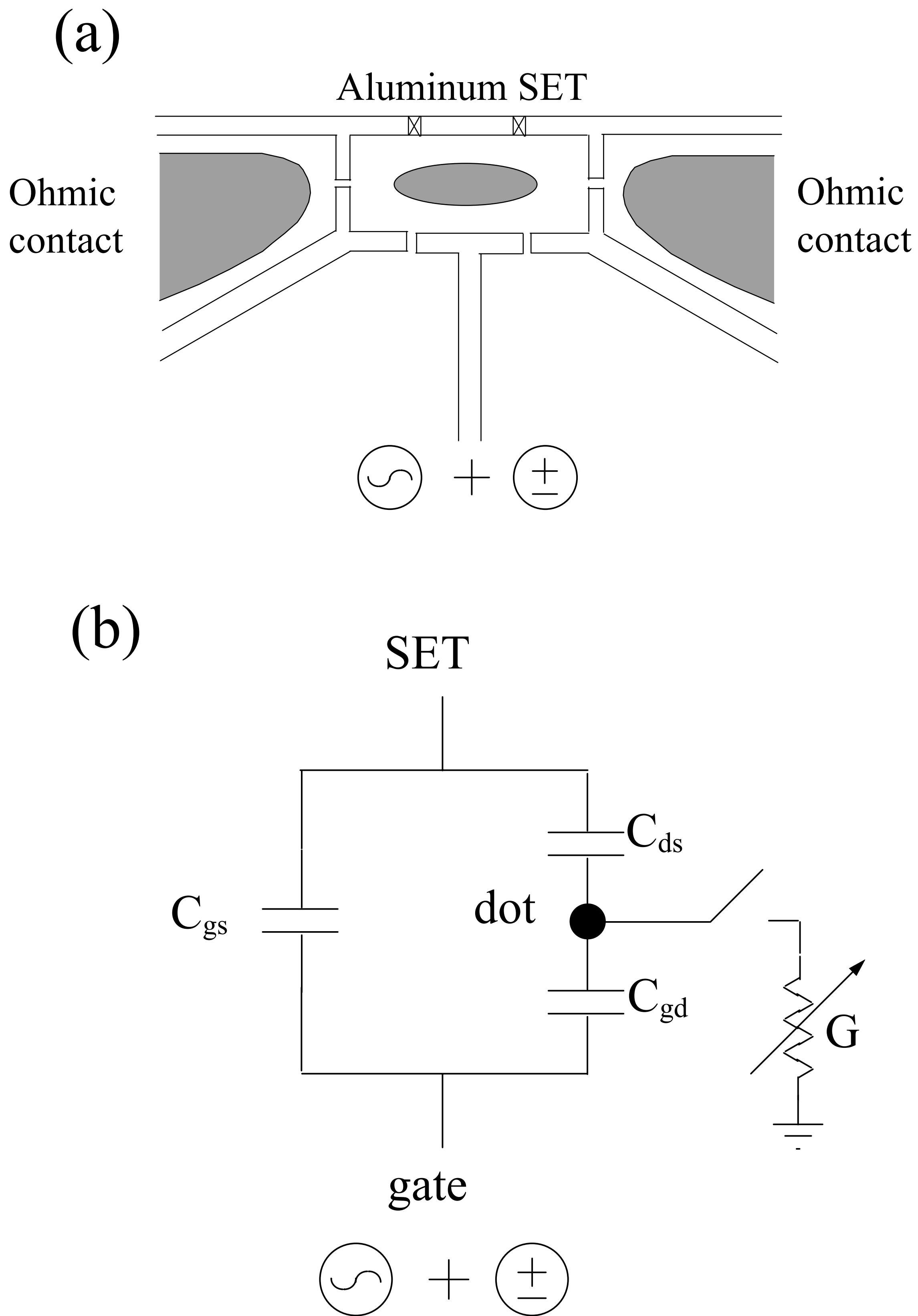


Figure 23. (a) Schematic of the sample used for the quantum fluctuations measurements. (b) Equivalent circuit of the sample with some of the physical quantities in the measurement setup.

Through application of a DC voltage, V_g, to the lead marked "gate" in Figure 21, charge can be drawn onto the dot as $eN = C_{gd}V_g$, where C_{gd} is the gate-dot capacitance as shown in the schematic in Figure 23. However, for zero temperature and for high tunneling barriers separating the dot from the leads, the charge on the quantum dot is quantized and can only change from n to n+1 around points in gate voltage, where $N = n + 0.5$. The measured quantum dot capacitance lineshape is $C_{meas} = e\frac{\partial \bar{n}}{\partial V_g}$, where $\bar{n}$ is the average number of electrons on the dot.

5.3 Measurement

The capacitance lineshape is measured by applying a small ac excitation (40μV *rms*, 1kHz) to the gate. This signal modulates the charge on the quantum dot by an amount that is a function of N and the coupling strength. The small ac modulation of the quantum dot charge induces ac charge on the SET central island resulting in a current through the SET at the excitation frequency. Examples of measured SET response as V_g is swept are shown in Figure 24 for three different tunnel coupling strengths. The upper trace is obtained for $G = 1.65\frac{e^2}{h}$, where $\bar{n}$ deviates only slightly from N and the electrostatic potentials in the dot and the leads are nearly equal. A prominent feature of this curve is an oscillation with a period of 94mV. This period arises due to an addition of one

electron to the SET central island through a direct capacitance $C_{gs} = 1.7\text{aF}$ to the gate, modulating the gain of the SET.

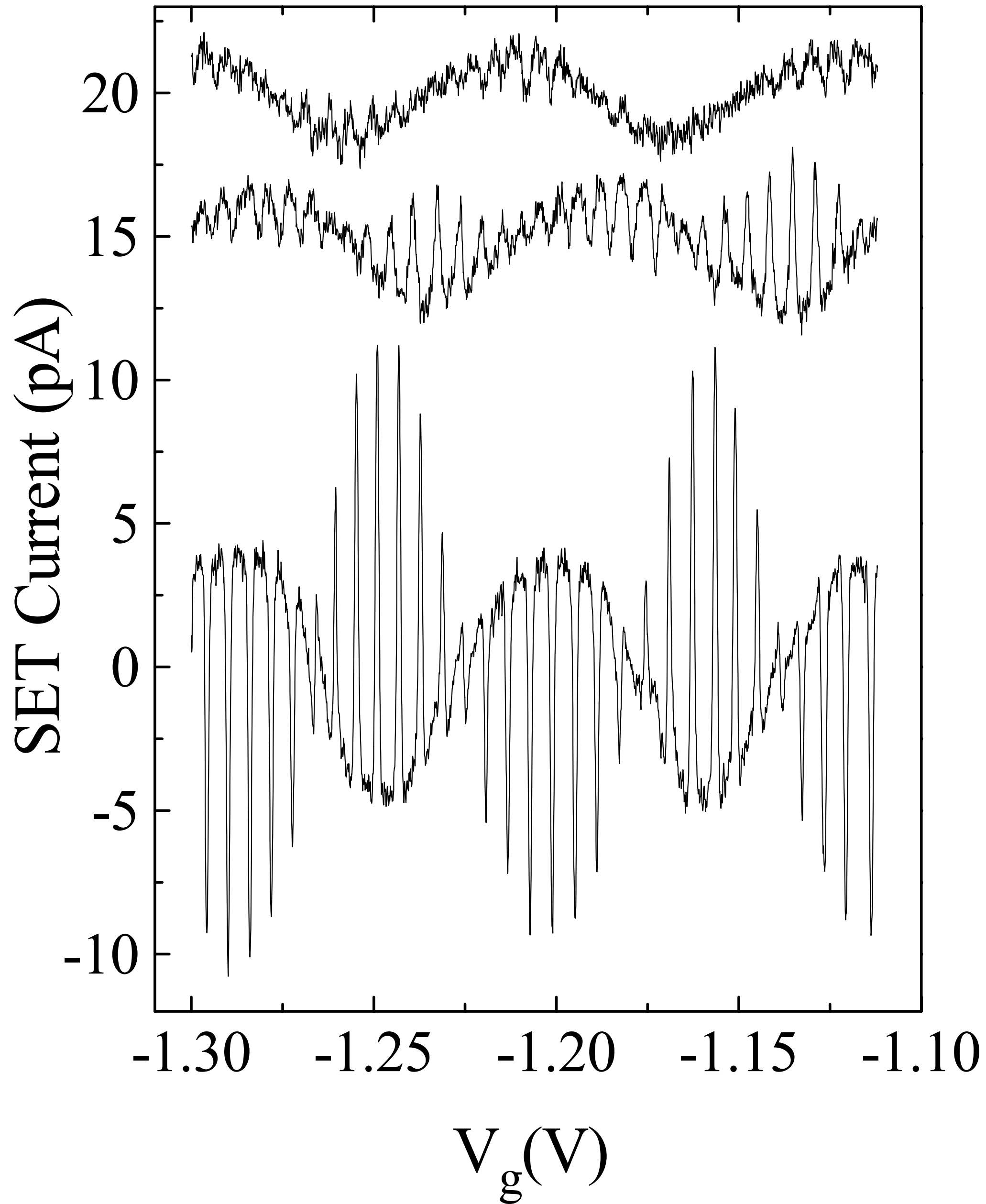


Figure 24. SET signal vs. gate voltage for three values of point contact conductance. Top to bottom: G=1.65, 1.32 and 0.05e^2/h.

The bottom trace in Figure 24 is obtained for $G = 0.05\frac{e^2}{h}$. Here, the charge on the dot is well quantized and can only change in close proximity to points where $N = n + 0.5$. These points correspond to the sharp peaks in the trace, spaced with a mean period of 6.3mV, yielding a gate-dot capacitance of $C_{gd} = 25\text{aF}$. Notice that the large-period background oscillation has a larger amplitude compared with the upper traces in Figure 24.

Between the peaks, the dot potential is effectively floating; charge cannot enter the dot from the reservoir to screen the ac gate potential. Thus, more charge is induced on the SET in response to the ac excitation on the gate because the ac coupling from the gate to the SET is augmented by a factor of $\frac{C_{gd}C_{ds}}{C_\Sigma}$. Here, C_{ds} is the quantum dot-SET central island capacitance and C_Σ is the total capacitance of the quantum dot.

In general, the charge response on the SET central island, dQ_{SET}, to the ac excitation on the gate, dV_g, can be expressed as:

$$dQ_{SET} = \left(\left(C_{gd} - C_{meas}\right)\frac{C_{ds}}{C_\Sigma} + C_{gs}\right)dV_g \qquad (1)$$

As our SET operates in the linear response regime, the current through the SET directly reflects dQ_{SET}. Linear response is ensured because the ratio of C_{ds} to the total capacitance

of the SET central island is about 0.05. Therefore, a change of charge of one electron in the quantum dot only induces $\frac{1}{20}^{\text{th}}$ of an electron on the SET. Moreover, we obtain our capacitance lineshapes at maximal gains of SET where this small induced charge has minimal effect on the SET gain. The reverse effect of the SET on the quantum dot charge is also very small. The ratio $\frac{C_{ds}}{C_{\Sigma}}$ is approximately 0.06, producing negligible feedback. Also, the charge on the SET central island is weakly quantized since a source-drain voltage is applied to the SET, which is $V_{ds} = \frac{E_c}{e}$, where E_c is the charging energy of the SET central island. Thus, the number of electrons on the central island of the SET fluctuates rapidly. Using equation (1), we extract the quantum dot capacitance lineshapes, $C_{meas}(V_g)$, from the raw data as a function of the tunnel barrier conductance.

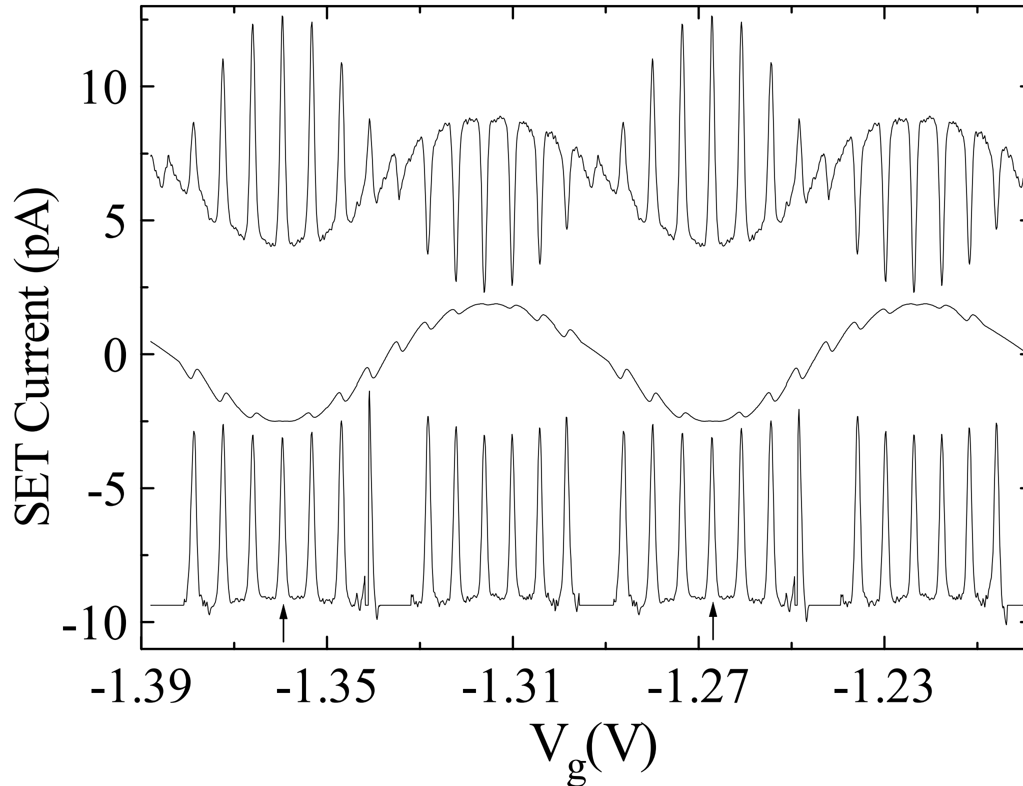


Figure 25. Process of isolation of quantum dot capacitance peaks from the variation of the SET gain with gate voltage. Top: SET signal for point contact conductance of approximately 0.01e^2/h. Middle: computed SET gain. Bottom: extracted quantum dot signal.

Figure 25 graphically shows the process of extracting the quantum dot peaks from the SET signal. The top curve is an example of the current through the SET for a relatively small point contact conductance. The middle curve is the computed gain of the SET as a function of the gate voltage. By dividing the SET signal by the SET gain, we obtain the true signal due to the quantum dot. The regions in the quantum dot signal corresponding to the zero crossings of the SET gain have been removed. This was done to reduce the large fluctuations in the resulting quantum dot signal due to the amplification of noise in the original SET signal when it is divided by zero. Notice that the lineshapes of the

quantum dot peaks that appear outside the maximal gain regions are slightly distorted. As discussed in Chapter 3, the SET gain is inherently nonlinear. The response of the SET current to this AC excitation can be expressed as: $I_{SET} = AV_{ac}$. Here, A is the gain, which is proportional to the slope of the I_{ds}-V_{gs} relationship. Clearly, A is not a linear function of the DC gate voltage, V_g. The gain, A, of the SET can be Taylor expanded as: $A = \alpha V_g + \beta V_g^2 + \ldots$ The condition of linearity states that $\alpha V_g >> \beta V_g^2$. So, we aim to utilize the SET in a linear regime by using the smallest possible amplitude for the AC excitation voltage. On the other hand, reducing the amplitude of the AC excitation decreases the signal-to-noise ratio. So, we maintain the amplitude of the AC signal, V_{ac}, such that linearity holds at least in regions of high gain. Therefore, in our lineshape analysis, we use only the undistorted peaks centered directly at points of maximum gain of the SET. These peaks are pointed out by arrows in Figure 25.

5.4 Capacitance lineshape results

For high tunneling barriers, the lineshape of the quantum dot capacitance peak as a function of gate voltage, $C_{meas}(\mathrm{V}_g)$, is very well described by a derivative of the Fermi function: $C_{meas} = C\left(\cosh\left(\frac{C_{gd}}{C_\Sigma}\frac{\mathrm{eV_g}}{2\mathrm{k_B}T}\right)\right)^{-2}$, where V_g varies from $-e/2C_{gd}$ to $+e/2C_{gd}$. The full width at half maximum of these peaks in gate voltage is: $FWHM = \frac{1}{e}\frac{C_\Sigma}{C_{gd}}\left(3.52k_BT\right)$.

After extracting the quantum dot capacitance peaks from the SET signal, we determine the total capacitance of the quantum dot, C_Σ, from the slope of the temperature

dependence of the linewidth for high tunneling barriers, which is $3.52\frac{C_\Sigma}{C_{gd}}\frac{k_B}{e}$. Figure 26 shows the dependence of the full width at half maximum of a quantum dot capacitance peak on the refrigerator temperature. At high temperatures, the dependence of the full width at half maximum is linear. The slope of the dependence is 4.13mV/K, yielding a total capacitance of $C_\Sigma = 340\text{aF}$, with a charging energy of $U = \frac{e^2}{2C_\Sigma} = 0.23\text{meV}$. For low temperatures, the dependence is relatively flat, because the electrons in the sample generally cannot be cooled to the base refrigerator temperature. Stray electromagnetic radiation, room temperature heating propagating down the coaxial cables, current through the transistor and various other phenomena increase the electron temperature above the refrigerator temperature. The crossover from the linear temperature dependence to the saturation region occurs at a refrigerator temperature of approximately 0.2K.

By fitting the capacitance peaks with the highest tunneling barriers with a Fermi function derivative, we obtained a finite electron temperature of about 0.13K. In our temperature dependence measurements we obtained a saturation temperature higher than the temperature from the Fermi function fit. This can be explained by the fact that the capacitance peak which was used in the temperature dependence measurements was not obtained for the highest tunnel barriers, and there was some residual broadening from the increased coupling between the dot and the reservoir. This is evident in the extrapolation of the fit in the linear regime to zero temperature, which corresponds to a finite peak width of about 0.55mV. For the highest tunneling barriers, this width should be zero.

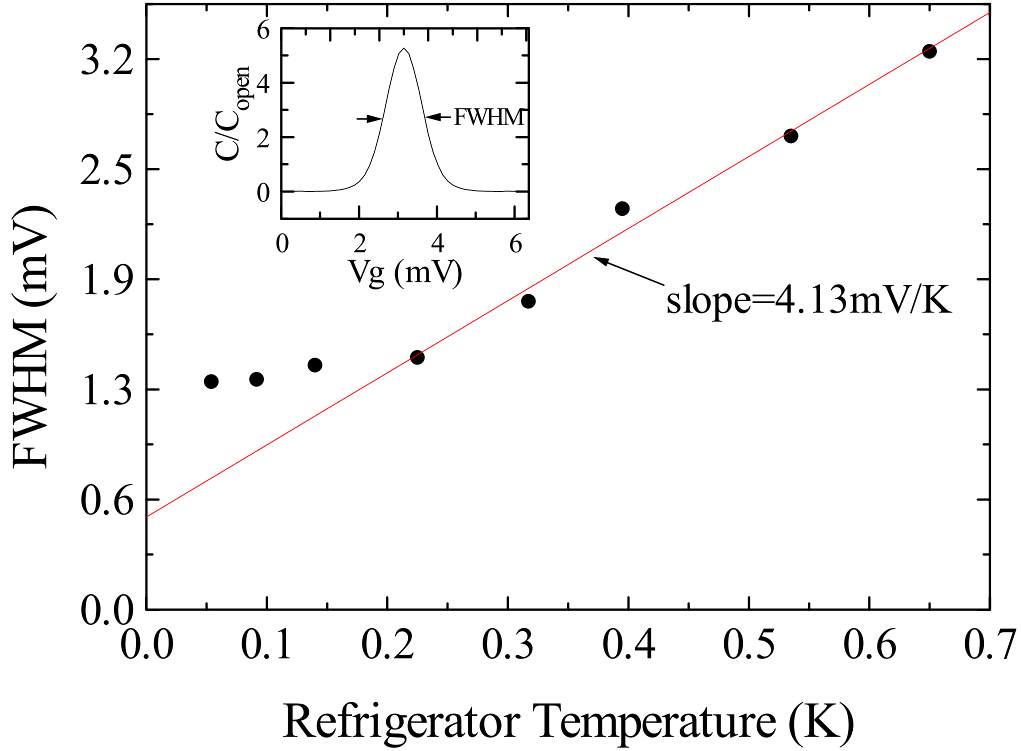


Figure 26. Temperature dependence of the full width at half maximum (FWHM) of a capacitance peak obtained with high tunneling barriers. The slope of the dependence is: $\mathrm{slope} = 3.52 \frac{C_\Sigma}{C_{gd}} \frac{k_B}{e} = 4.13$ **mV/K. The inset shows the peak for a temperature of T=0.05K with the value of the full width at half maximum denoted by arrows.**

To deplete the electrons underneath the metal leads, it is necessary to apply a negative DC voltage to the leads relative to the two-dimensional electron gas. To avoid applying large DC voltages to the highly delicate single-electron transistor, we apply a positive DC voltage of +0.57V to the 2DEG. In the following discussion, we will refer to point contact voltages in terms of values relative to the 2DEG. During the measurement of the capacitance lineshapes, point contact 2 is completely pinched off by setting the bias on the defining lead at -0.745V relative to the 2DEG. This isolates the effect of the

conductance of point contact 1 on the capacitance lineshape of the quantum dot. This is done because of the high electrostatic coupling between point contacts 1 and 2. For example, changing the voltage on point contact 1 not only varies the conductance through contact 1, but also significantly alters the conductance of contact 2. The drawback of performing the measurement in this manner is that it is impossible to measure the capacitance lineshape and the conductance simultaneously. To determine the conductance of contact 1 in this regime, we perform the following procedure. The conductance of contact 1 is measured with the voltage on point contact 2 set to zero volts relative to the 2DEG, so it is completely open. To account for the change in conductance of point contact 1 due to the electrostatic coupling from contact 2, we monitor the shift of conductance plateaus of contact 1 as 2 is being closed. This procedure allows us to extrapolate G, the conductance of contact 1, to the regime of the capacitance measurement. Figure 27 shows that we were able to observe a shift in the conductance of point contact 1 by changing the voltage on point contact 2 from 0 to -0.186V relative to the 2DEG. By extrapolating this shift to the value of -0.745V on point contact 2, we obtain the expected conductance of point contact 1 during the measurement of capacitance lineshapes. Actually, by slightly depleting the 2DEG underneath point contact 2, we inevitably introduce a series resistance with the tunnel barrier of point contact 1. To determine the actual conductance of point contact 1, we account for this series resistance by subtracting it from the measurement. As the series resistance due to point contact 2 increases, its effect is more difficult to subtract. So, we are forced to use the shift from point contact 2 voltage bias of 0V to -0.186, and extrapolate it to the point contact 2 voltage bias of -0.745. This is a rather large extrapolation, but it turns out to be

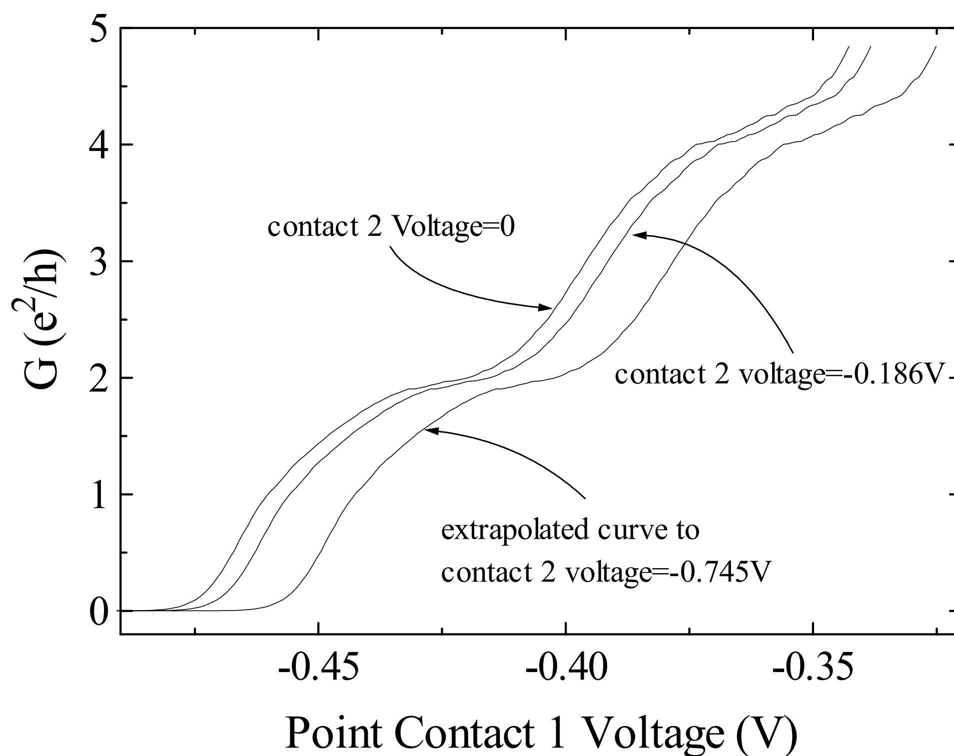


Figure 27. Shift in the conductance of point contact 1 due to the voltage on point contact 2. The curves for contact 2 voltages of 0 and -0.186V relative to the 2DEG are measured. The curve for contact 2 voltage of -0.745V is the curve with the extrapolated shift from the other two curves.

a fairly good one, judging from the comparison of the expected values of tunnel barrier conductance to the values extracted from the calculated capacitance lineshape fits, as shown in Figure 34.

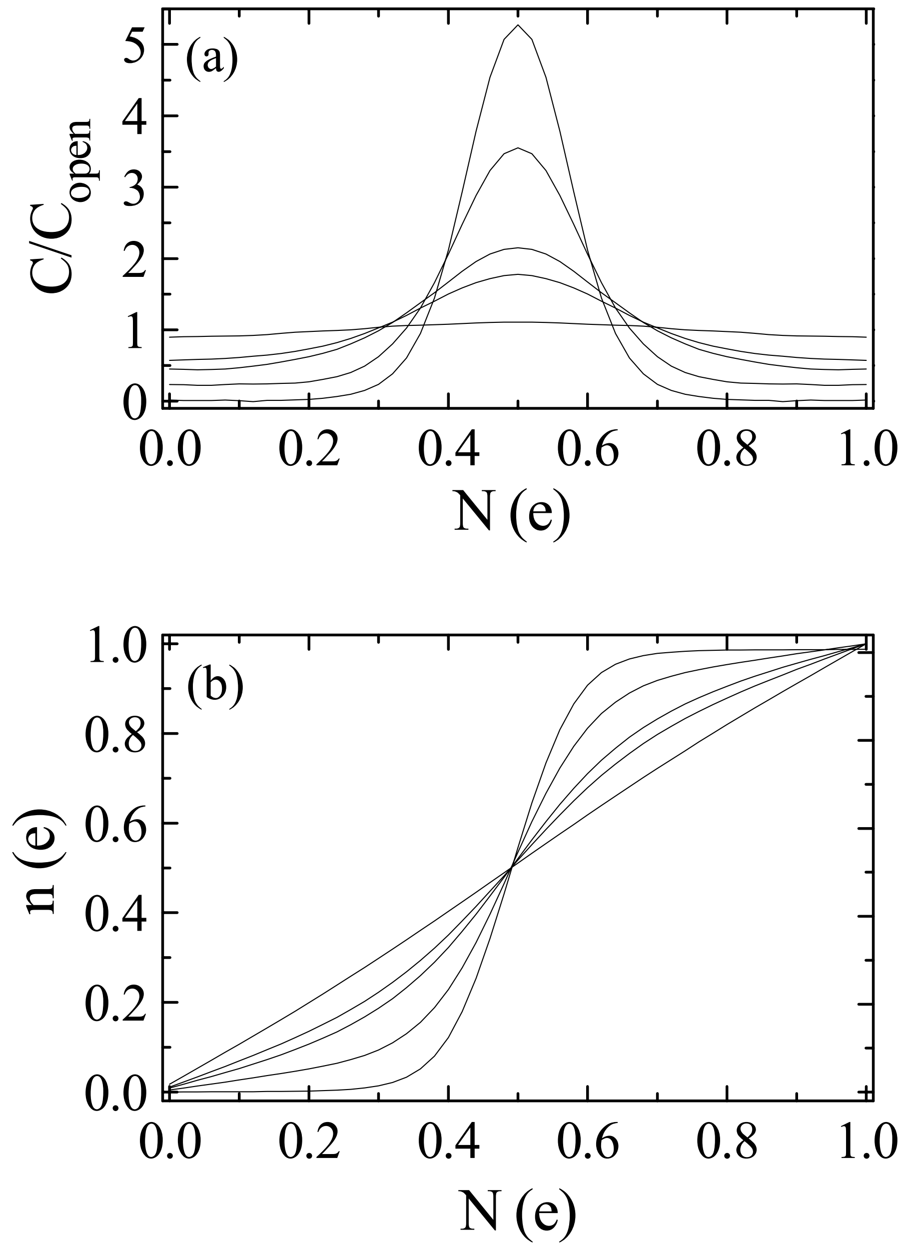


Figure 28. (a) Five capacitance peaks with varying point contact conductance. G=0.010, 0.67, 1.09, 1.50 and 1.81 e^2/h. (b) The variation of the number of electrons, *n*, on the quantum dot with the gate charge, *N*, for different point contact conductance. Each trace corresponds to the integral of the curve in (a).

Figure 28a shows the evolution of the capacitance lineshape with increased coupling strength. The nominal values of G are: 0.010, 0.67, 1.09, 1.50 and $1.81\frac{e^2}{h}$. It is clear that as G increases and approaches $\frac{2e^2}{h}$, the capacitance peaks broaden and the Coulomb blockade oscillations diminish and disappear.

In Figure 28b, we show the number of electrons on the quantum dot, n, as a function of the gate charge, N. Each curve in Figure 28b corresponds to an integral of the curve in Figure 28a. For each trace of n, the sum of one electron is conserved. As the point contact conductance, G, increases toward $2e^2/h$, n deviates from the limit of a sharp step and approaches a straight line with a slope of 1. Below, we discuss the lineshapes of different quantum dot capacitance peaks in various coupling regimes: very weak, weak and strong.

In the very weak coupling regime, the shape of the capacitance peak is determined simply by thermal broadening. Figure 29 shows good agreement between a peak measured with $G = 0.010\frac{e^2}{h}$ and a derivative of the Fermi-Dirac function for a temperature of T=0.13K. There is a slight difference between the fit and our data at the corners of the curve, for N=0.3 and 0.7*e*. We propose that this deviation is due to a slight nonlinearity of the SET amplifier. The amplifier nonlinearity is caused by a deviation from a straight line of the SET gain within the amplitude of the AC excitation, which is 40μV. We have modeled

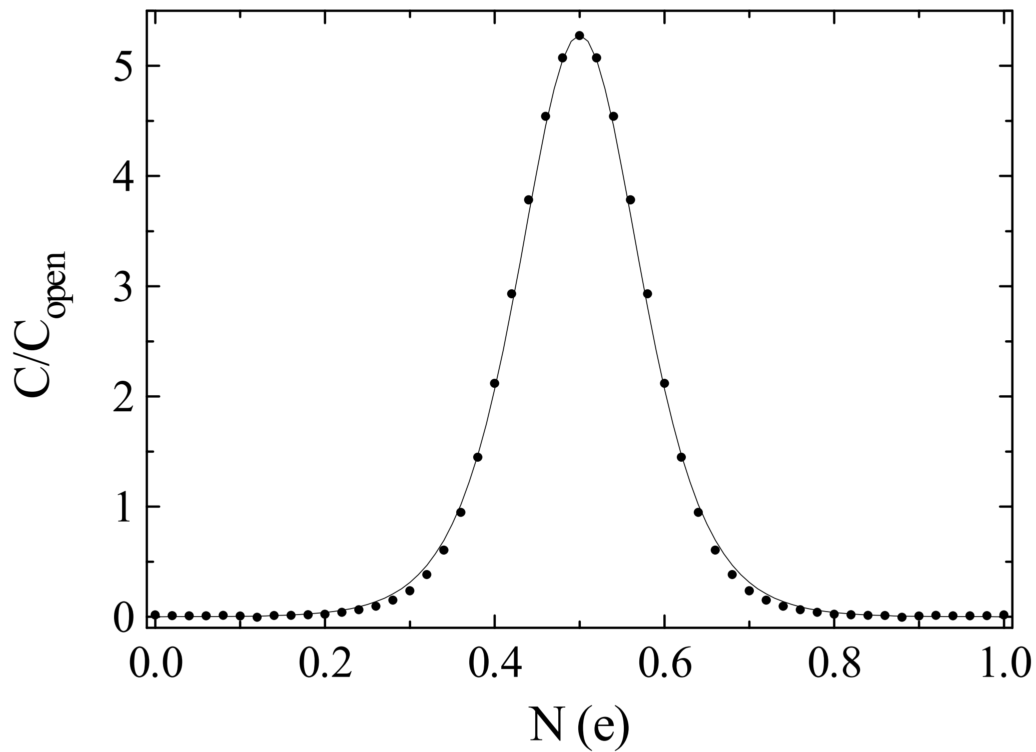


Figure 29. Filled circles: capacitance peak obtained with a point contact conductance of G=0.010e^2/h. Straight line: Fermi-Dirac function derivative with T=0.13K.

our amplifier and used a Taylor expansion of the transfer function to determine the significance of the higher order terms in the gain. It turns out that the coefficient of the second order term in the expansion is about 15 times smaller than the first order term. This is a very small contribution, but it could explain the slight deviation from the fit.

For larger tunnel barrier conductance, the capacitance lineshape changes. In Figure 30a, b, c and d, we plot with open circles capacitance peaks that we obtained for nominal values of G=0.67, 1.09, 1.50 and $1.81\frac{e^2}{h}$. We compared our capacitance peaks with expressions that have been previously used to fit conductance peaks. For example, Lorentzian lifetime broadening has been considered [5-9], as in equation (2), for characterizing the charge smearing effects.

$$C = A\cosh^{-2}\left(\frac{E}{2k_B T}\right)\otimes\frac{(\Gamma/2)\pi}{(\Gamma/2)^2+\left(eV_g\, C_{gd}/C_\Sigma + E\right)^2} \qquad (2)$$

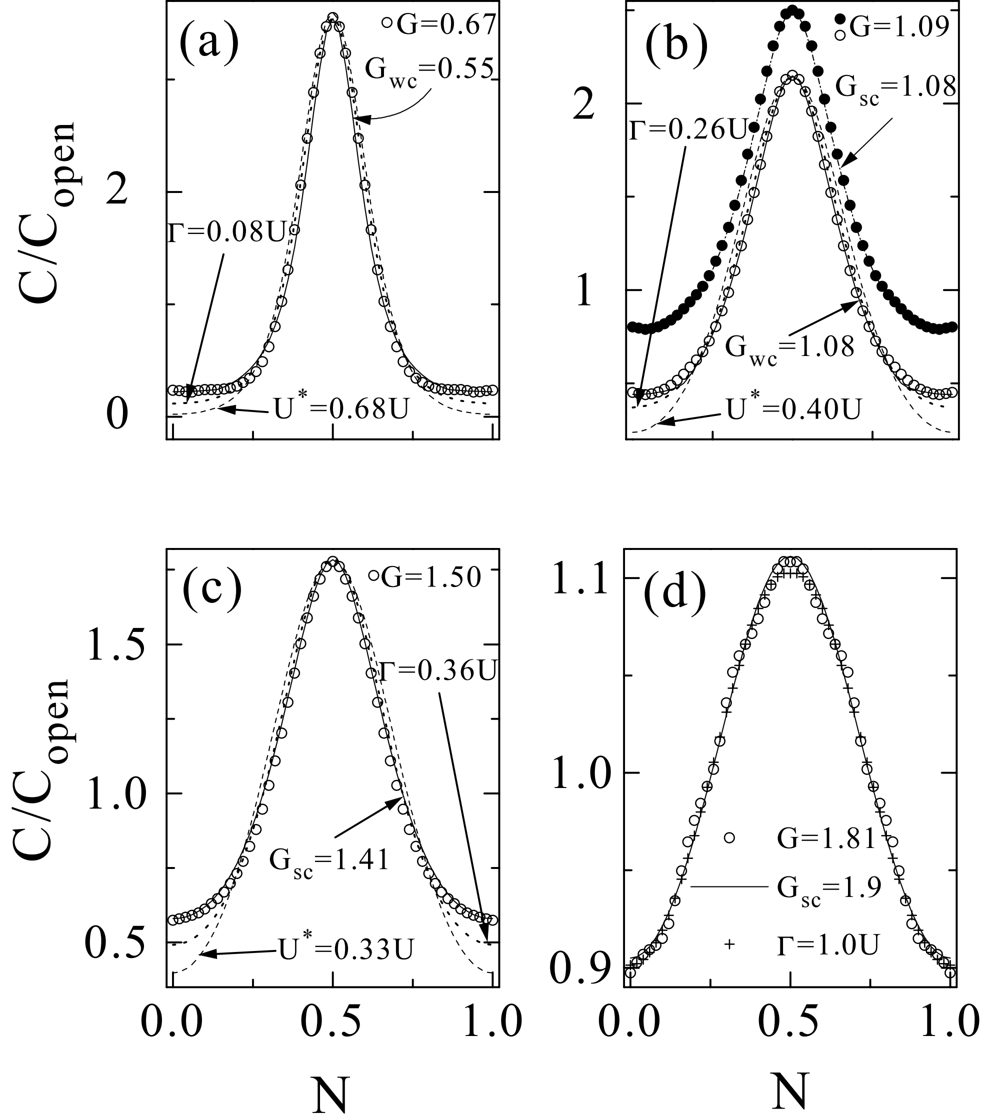


Figure 30. Capacitance peaks for increased tunnel coupling. (a) Open circles: data for G=0.67e^2/h, solid line: fit to weak coupling theory (wc) with G_{wc}=0.55e^2/h, dotted line: Lorentzian with Γ=0.08U, dashed line: derivative of the Fermi function with U^*=0.68U. (b) Open circles: data for G=1.09e^2/h, solid line: wc fit with G_{wc}=1.08e^2/h, dotted line: Lorentzian with Γ=0.26U, dashed line: derivative of the Fermi function with U^*=0.40U. Closed circles: data for G=1.09e^2/h offset by 0.35 vertically, dash-dot line: strong coupling theory (sc) fit with G_{sc}=1.08e^2/h. (c) Open circles: data for G=1.50e^2/h, solid line: sc fit with G_{sc}=1.41e^2/h, dotted line: Lorentzian with Γ=0.36U, dashed line: derivative of the Fermi function with U^*=0.33U. (d) Open circles: data for G=1.81e^2/h, solid line: sc fit with G_{sc}=1.90e^2/h, crosses: Lorentzian with Γ=1.0U.

In Figure 30a, the lower plot of Figure 30b, Figure 30c and d, we plot Lorentzian-broadened Fermi peaks with energy level widths Γ=0.08, 0.26, 0.36 and 1.0U. The lineshapes show significant deviations from the data. We have obtained these values by using a least-squares fit to our data. The largest mismatch between our data and this calculation is at the valleys of the peaks.

Previous measurements of charge fluctuations used a renormalized quantum dot charging energy U^* to account for peaks broadened with a finite tunnel barrier conductance [5-12]. In Figure 30a, b and c, we plot derivatives of the Fermi function with U^*=0.68, 0.40 and 0.33U for a temperature of 130mK. The mismatch between our data and these peaks is also largest. This mismatch is even greater than with the Lorentzian-broadened peaks.

Finally, we compared our experimental results to the theoretical treatment developed by Matveev [5-7][5-8]. The problem of interaction between the dot and the leads was solved in the limits of weak [5-6][5-7] and strong [5-8] coupling using either transmission or reflection of the tunnel barrier as a small parameter in perturbation theory. In both limits, the physics of charge fluctuations is related to spin fluctuations in the Kondo problem. Here, instead of the degeneracy of the two-spin states, there is a degeneracy between the dot states with n and n+1 electrons. Similarly to the Kondo effect [5-19], the charge displays a logarithmic divergence around these degeneracy points at very low temperatures [5-7] [5-8]. As a result, the predicted capacitance lineshape has more

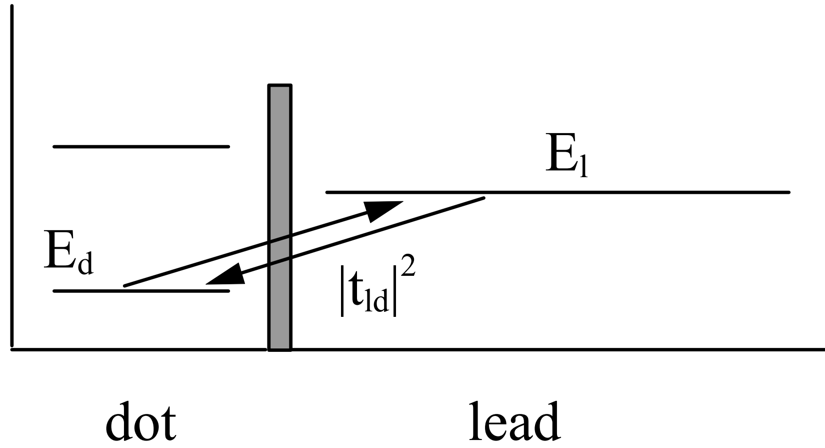


Figure 31. Schematic of the weak coupling perturbation theory. Tunnel coupling between states E_d in the dot and E_l in the lead is considered. The capacitance lineshape is calculated by summing the total contribution from coupling between all possible states in the dot and the lead.

weight around the half integer values of *N* in comparison with other theoretical treatments.

For weak coupling, in the range of $G_{wc} << \frac{2e^2}{h}$, Matveev determines the peak shape by treating the tunnel coupling between the quantum dot and the reservoir as a perturbation. He considers the virtual tunneling events of an electron from an energy state E_l in the lead to an energy state E_d in the dot and back to the reservoir. The capacitance lineshape is calculated by summing the total contribution from coupling between all possible states in the dot and the lead. Figure 31 shows a schematic of this process. This second order correction to the charge can be written as [5-6][5-7]:

$$Q = aeG_{wc}\left(\frac{h}{4\pi^2 e^2}\right)\ln\frac{0.5+N}{0.5-N} \tag{3}$$

The capacitance peak can be obtained by differentiating the charge:

$$C = \frac{\partial Q}{\partial V_g} = aC_{gd} G_{wc} \left(\frac{h}{4\pi^2 e^2} \right) \left(\frac{1}{0.5 - N} + \frac{1}{0.5 + N} \right) \tag{4}$$

The above expression is derived in the interval -0.5 < N < 0.5 and in the theory [5-7], a=1.. Near the peak centers, where $N = \pm 0.5$, this expression diverges. Therefore, Matveev's theory for non-zero temperatures yields an expression for the quantum dot charge with a Fermi-Dirac component and a correction that is linearly dependent on G_{wc} [5-20]:

$$Q = \frac{E_c}{2k_B T} \left\{ 0.5 * (1 - \tanh u) - G_{wc} \tanh u \left(\ln \frac{E_c}{u \coth u} + 1 \right) \right\} -$$

$$\frac{E_c}{2k_B T} G_{wc} \int_0^\infty \frac{\sinh t}{t^2} \left(\frac{t - u}{\sinh(t - u)} + \frac{t + u}{\sinh(t + u)} \right) - \frac{2 \sinh u}{t + u \coth u} dt$$

Here, $u = \frac{E}{k_B T}$ and G_{wc} is the value obtained from fitting the weak coupling expression in the valleys of the peaks. The capacitance lineshape can be obtained from this expression by taking the derivative of the charge: $C = \frac{\beta}{k_B T} \frac{\mathrm{d}Q}{\mathrm{du}}$. Here, β is the lever arm: $\beta = \frac{C_\Sigma}{C_{gd}}$.

In Figure 30a and the lower plot of Figure 30b, along with our data, we show capacitance peaks obtained with the weak tunneling perturbation theory for tunnel barrier conductances of G_{wc}=0.55 and 1.08e^2/h. These peaks are in excellent agreement with our data that was obtained with tunnel barrier conductances of G=0.67 and 1.09e^2/h. We

found that on average, G_{wc} corresponds to G if a=4, rather than 1, as in the theory. A similar discrepancy was found elsewhere [5-21], but its cause is not known at this time.

The weak coupling theory is derived for $G_{wc} << \frac{2e^2}{h}$, but it works surprisingly well for capacitance peaks with a tunnel barrier conductance as high as $1.09e^2/h$, as shown in Figure 30b. For higher values of G, it is necessary to use a different formulation.

In the limit of high G, where it is just below $2e^2/h$, the quantum dot can be treated as a small charge perturbation on the two-dimensional Fermi liquid. In the spinless case, this perturbation creates Friedel oscillations, forming a charge density wave in space of the form $\rho(x) = ek_F \cos(k_F x - \phi)$, where k_F is the Fermi wavevector [5-22]. Since the tunnel barriers can be regarded as one-dimensional, the perturbation can also be treated in one dimension. By polarizing the charge on the dot, the effect of changing the voltage on the gate electrode is to push or pull electrons into and out of the dot. Therefore, the phase of the charge density wave is: $\phi = 2\pi \frac{C_{gd}V_g}{e} = 2\pi N$, where C_{gd} is the capacitance coupling the gate electrode and the quantum dot, and V_g is the voltage on the gate. By assuming that the potential of the tunnel barrier is of the form $V(x) = r\delta(x)$, where r is a coefficient of reflection from the barrier, and $\delta(x)$ is a delta function, the first order correction to the ground state energy is:

$$\delta E_1 = \int \rho(x)V(x)dx = rE_c \cos(2\pi N) \tag{5}$$

This perturbation theory relies on the fact that the reflection r^2, which is related to the tunneling barrier conductance as $G_{sc} = \frac{2e^2}{h}\left(1-r^2\right)$, is small.

The above description is given for electrons without spin. To treat the case of electrons with spin in the nearly open regime, Matveev must use higher orders of perturbation theory, because the first order correction vanishes with the introduction of unpinned fluctuations in the spin channel. This correction to the ground state energy is given as [5-8]:

$$\delta E = -br^2 E_c \ln\left(\frac{1}{r^2\cos^2\pi N}\right)\cos^2\pi N \tag{6}$$

The capacitance correction can then be extracted from the energy according to: $C = \frac{\partial^2 E}{\partial V_g^2}$, giving the result:

$$C(N) = bC_{gd}r^2 \ln\left(\frac{1}{r^2\cos^2\pi N}\right)\cos 2\pi N \tag{7}$$

The above expression is not normalized, and it gives the deviation of the capacitance C from 0. It is necessary to add a constant C_0 that is established by setting the integral of *C(N)* equal to one electron. In the theory, *b*=2.27. The logarithmic divergence is analogous to a similar behavior of magnetic susceptibility in the two-channel Kondo problem [5-19]. To account for a finite temperature, the singularity in equation (7) is cut off by replacing $r^2\cos^2\pi N$ with $r^2\cos^2\pi N + \frac{k_B T}{U}$. The corrected expression was used for the fits.

In the top plot of Figure 30b, and in Figure 30c and d, we show capacitance peaks obtained with tunnel barrier conductances of 1.09, 1.50 and $1.81e^2/h$, respectively. The top plot in Figure 30b is offset by 0.35 for clarity. These figures also show the capacitance calculations of the strong coupling perturbation theory for tunnel barrier conductances of G_{sc}=1.08, 1.41 and $1.9e^2/h$, respectively, which have been obtained by fitting to our data by least squares optimization. There is excellent agreement all along the entire curves between our data and these theoretical calculations. Both the weak and strong coupling theories fit well to the capacitance peak in the intermediate coupling regime, obtained for G=$1.09e^2/h$. In Figure 30d, where we show a capacitance peak, obtained for a nearly completely transparent tunnel barrier conductance of $1.81e^2/h$, the shape of the capacitance is indistinguishable from a sinusoid. In this regime, it is difficult to discern any significant differences between any of the theoretical calculations. We found that the coefficient b=1, rather than 2.27, as in the theory, to maintain the dependence of the capacitance lineshape on G_{sc} in this regime. We do not know the reason for this discrepancy.

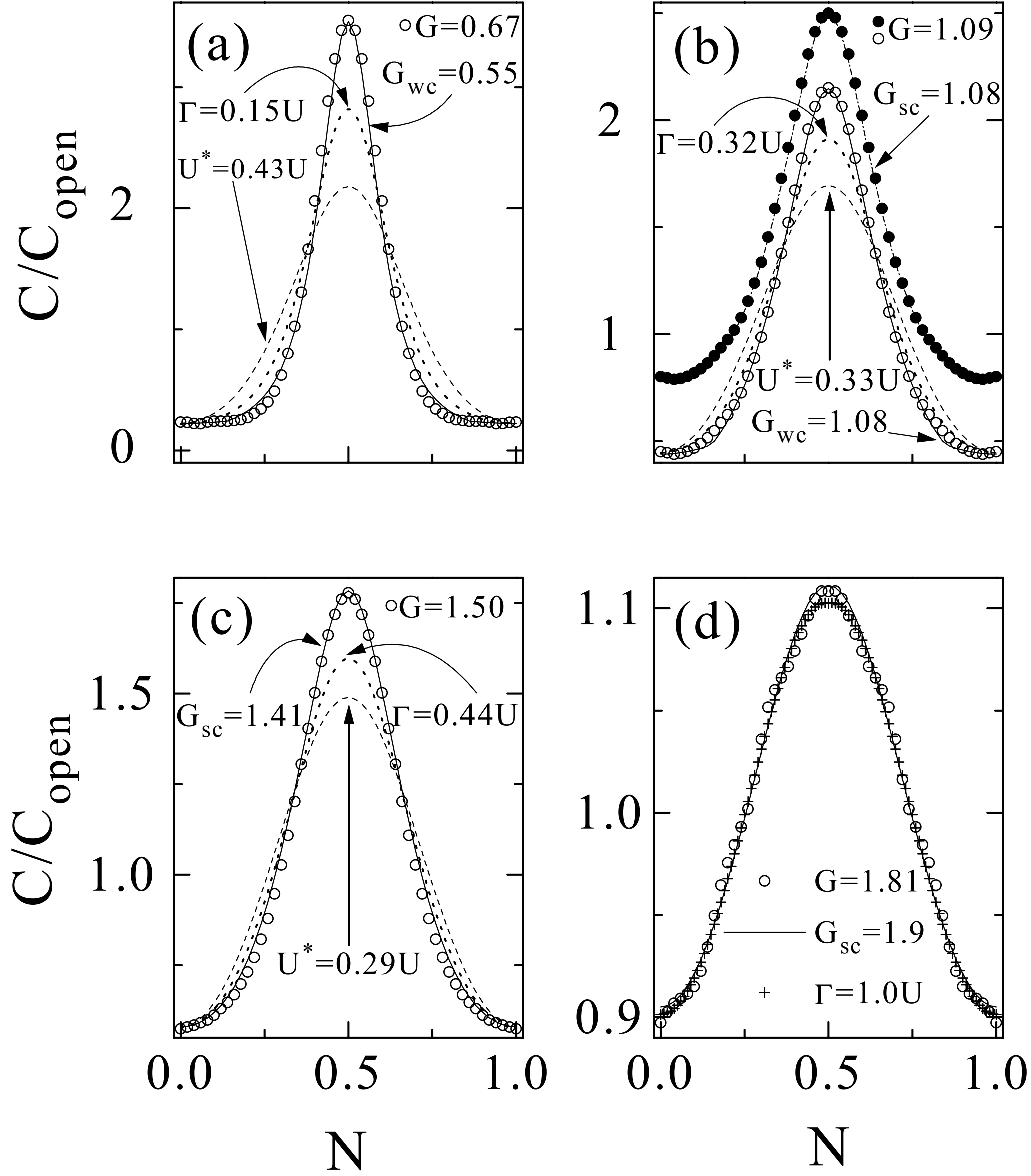


Figure 32. Capacitance peaks for increased tunnel coupling. (a) Open circles: data for G=0.67e^2/h, solid line: fit to weak coupling theory (wc) with G_{wc}=0.55e^2/h, dotted line: Lorentzian with Γ=0.15U, dashed line: derivative of the Fermi function with U^*=0.43U. (b) Open circles: data for G=1.09e^2/h, solid line: wc fit with G_{wc}=1.08e^2/h, dotted line: Lorentzian with Γ=0.32U, dashed line: derivative of the Fermi function with U^*=0.33U. Closed circles: data for G=1.09e^2/h offset by 0.35 vertically, dash-dot line: strong coupling theory (sc) fit with G_{sc}=1.08e^2/h. (c) Open circles: data for G=1.50e^2/h, solid line: sc fit with G_{sc}=1.41e^2/h, dotted line: Lorentzian with Γ=0.44U, dashed line: derivative of the Fermi function with U^*=0.29U. (d) Open circles: data for G=1.81e^2/h, solid line: sc fit with G_{sc}=1.90e^2/h, crosses: Lorentzian with Γ=1.0U.

By using a least-squares method of fitting the renormalized charging energy and the Lorentzian-broadened peaks to our capacitance lineshape data, the greatest discrepancy between our data and these approaches is between the centers of the peaks. We have observed that by selecting the parameters to fit these expressions in the peak valleys, the greatest discrepancy occurs at the centers of the peaks. Figure 32 shows the results of this different fitting approach.

Surprisingly, the renormalized charging energy approach [5-23] was derived with the same starting Hamiltonians as the perturbation theory. It seems that the authors of these calculations arrived at different answers by making different approximations in the solution of the problem. In deriving the renormalized charging energy theory, the author assumed that the contribution of the higher energy levels is negligible and concluded that the capacitance of the quantum dot can be renormalized. The perturbation theory calculation did not make this approximation and it therefore has more weight at the valleys of the peaks, possibly due to higher energy peaks.

The discussion above described lineshapes from a single sample from our measurements. We have performed these measurements on five other samples and observed similar results. The broadening of the quantum dot capacitance lineshape with increased coupling to the reservoir can be calculated with the perturbation theory methods described above. Figure 33 shows two examples of capacitance peak data obtained from another sample for two values of the tunnel barrier conductance. These peaks correspond very well to the calculated capacitance lineshape obtained with the strong coupling

theory described above for G_{sc}=0.99 and 1.37e^2/h. Unfortunately, the point contacts used in this sample did not display the quantized conductance steps as in Figure 27, so it is difficult to compare the values for G_{sc} with the expected values for the tunnel barrier conductance. The dependence of the characteristics of the point contacts on the shape of the leads defining them is discussed in Appendix B.

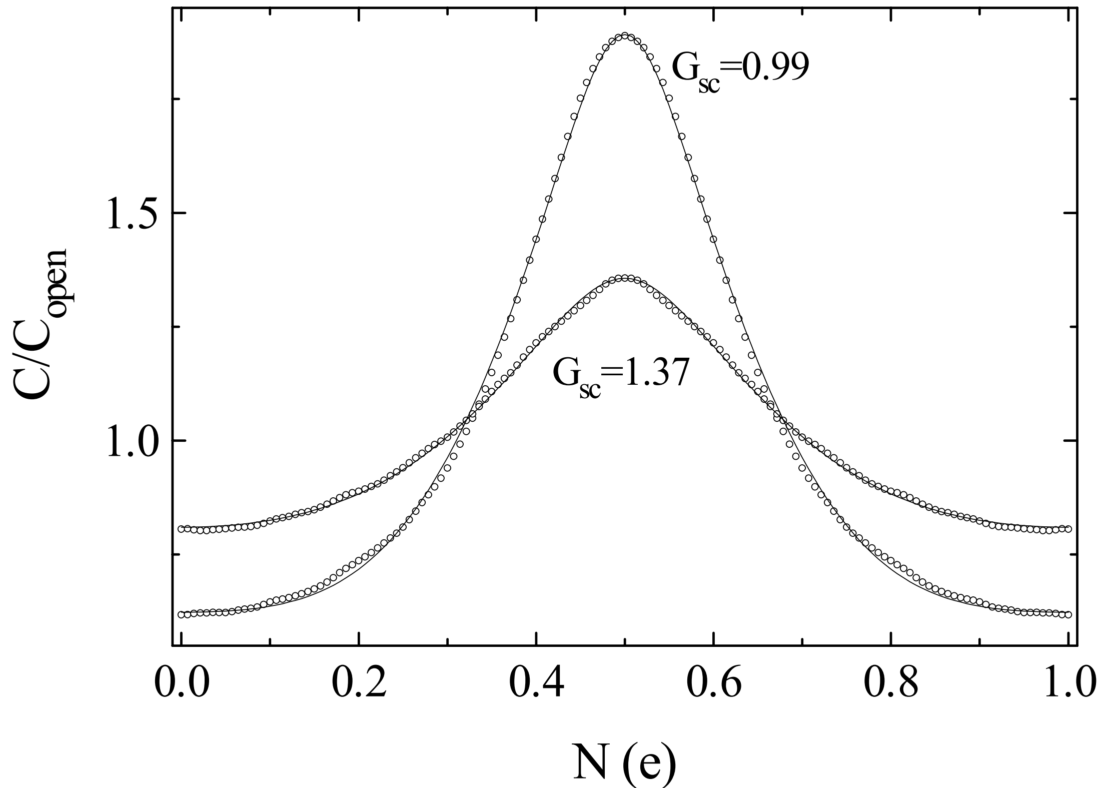


Figure 33. Comparison of capacitance peaks obtained on samples other than the one described above. Circles: capacitance measurement data obtained at T=43mK. Solid lines: capacitance peaks calculated with the strong coupling theory described above with G_{sc} =0.99 and 1.37e^2/h.

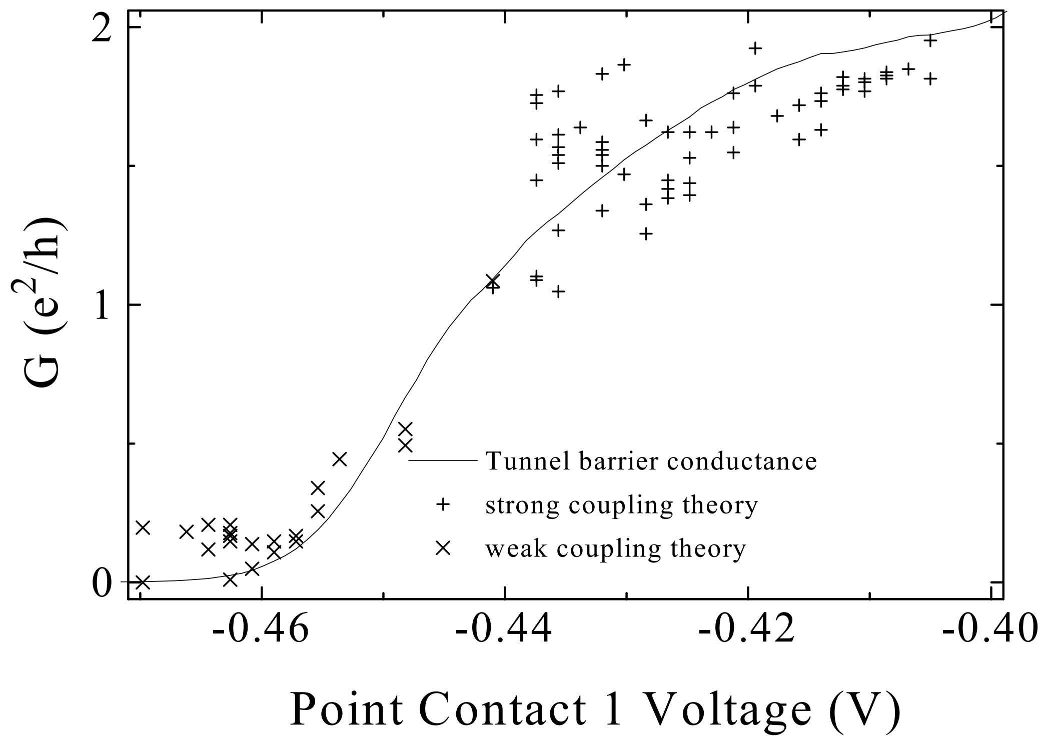


Figure 34. Tunnel barrier conductance of point contact 1 (solid line) vs. tunnel barrier lead voltage. ×: Conductance values obtained from fits with weak coupling theory (wc). +: Conductance values obtained from fits with strong coupling theory (sc).

Figure 34 shows the dependence of the tunnel barrier conductance of point contact 1 on the voltage of the lead defining the contact. We also plot the conductance values obtained from theoretical fits in the weakly and strongly coupled regimes. These values have large fluctuations around the measured tunnel barrier conductance. These fluctuations are a mystery that remains to be solved. They are seen consistently in all of our samples. Evidently, for a dot with a single point contact, the tunnel barrier conductance affecting the lineshape is different from the conductance through the dot which does not display comparable fluctuations.

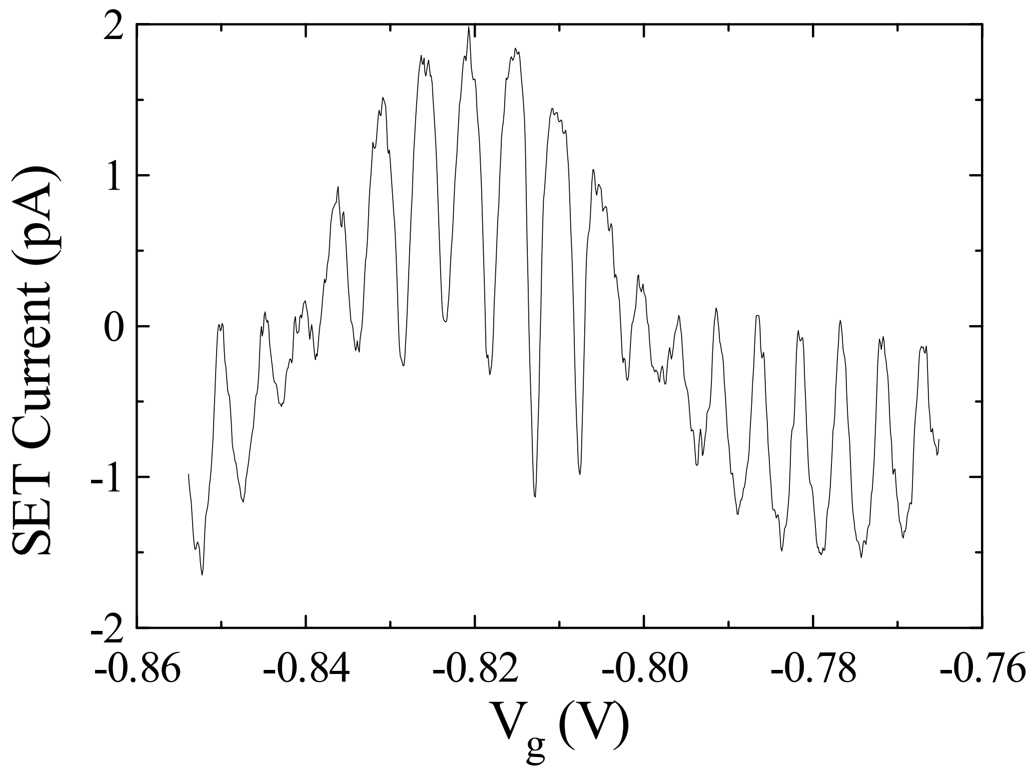


Figure 35. Scan of Vg showing an example of the fluctuations in the apparent value of the tunnel barrier conductance between different peaks.

Figure 35 shows an example of a sweep of V_g with large fluctuations in the apparent tunnel barrier conductance, even though the tunnel barrier conductance is held fixed during the sweep. We have observed such fluctuation in gate voltage sweeps for intermediate values of point contact conductance. In the very weakly coupled and strongly coupled regimes, these fluctuations are absent. Around values of $G=e^2/h$, the values of G_{wc} or G_{sc} are correlated over a few adjacent peaks. A similar effect was observed in conductance measurements in dots in the quantum Hall regime [5-24]. Theorists predict that such fluctuations can arise from quantum interference inside the dot

and should therefore be highly sensitive to magnetic field. This is consistent with results from *conductance* experiments [5-25] [5-26] [5-27]. There are similar theoretical predictions for fluctuations in capacitance peaks [5-22]. However, we observed no effect of magnetic field for magnetic fluxes through the dot as high as 30 flux quanta.

Figure 36 shows two gate voltage scans obtained at slightly different magnetic fields. The difference in flux through the quantum dot between the top and bottom scan is 30 flux quanta, and the character of the peak-to-peak fluctuations is not affected. The signal-to-noise ratio in this figure is worse because the gain of the SET amplifier is degraded by using it in the normal state, rather than in the superconducting state.

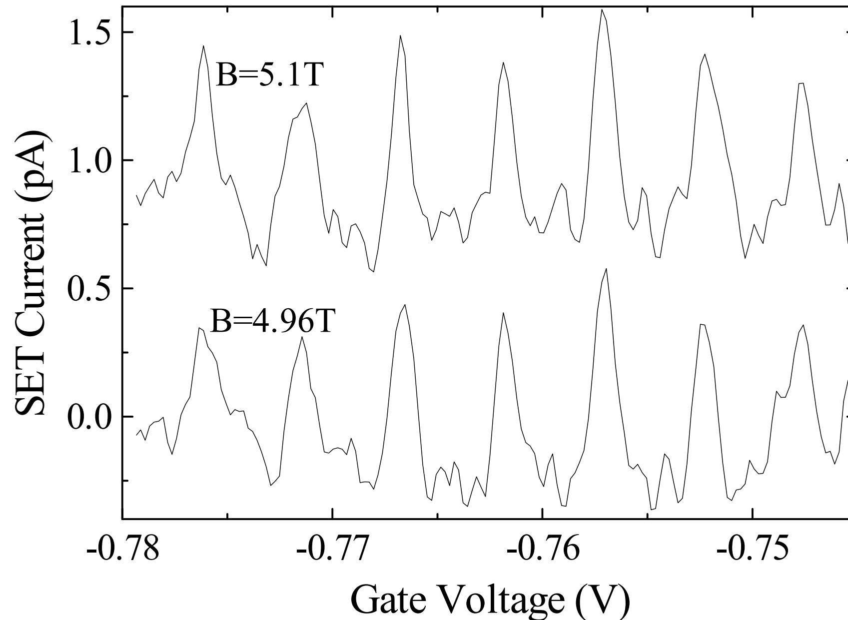


Figure 36. Varying the magnetic field through the quantum dot does not change the peak-to-peak fluctuations. The difference in flux through the quantum dot between the top and bottom scans is 30 flux quanta.

5.5 Magnetic field dependence

All of the capacitance lineshape data presented in the previous section was taken with a zero magnetic field through the sample. At zero field, the aluminum single-electron transistor is in the superconducting state and the gain of the device is much larger than in the normal state. Thus, to obtain a higher signal-to-noise ratio in our measurements, we performed them at zero magnetic field. In this regime, electrons in the quantum dot can exist in two spin states, and the capacitance lineshapes that we obtained agree very well with Matveev's theory derived for a quantum dot system with spin. To determine whether the system behaves differently in state in which the spins of all the electrons are aligned parallel to each other, we applied an external magnetic field, hoping to force the electrons in the quantum dot in a single spin state. Figure 37 shows the effect of scanning the magnetic flux through the quantum dot on the gate voltage sweeps. The shade of the gray scale image corresponds to the magnitude of the AC signal through the SET. Light regions correspond to a high signal, while dark regions correspond to a small signal. The vertical axis in Figure 37 corresponds to the gate voltage. The narrow, closely spaced horizontal stripes in the plot are the traces of the quantum dot single-electron peaks, while the wide horizontal bands correspond to the SET envelope. The traces of the quantum dot peaks in Figure 37 are fairly horizontal, except for a dip at a magnetic flux density of 4.88T.

In measurements on a bulk sample from this heterostructure, it was determined that the electron concentration is $n_e = 1 \times 10^{11}\,\mathrm{cm}^{-2}$, corresponding to a Landau level filling factor of ν=1 at $B_{\nu=1} = n_e \frac{hc}{e} = 4.14 \times 10^4\,\mathrm{Gauss}$ in CGS units or $B_{\nu=1}$=4.14T in MKS. Since the electron concentration in the quantum dot is probably different than in a bulk sample, the

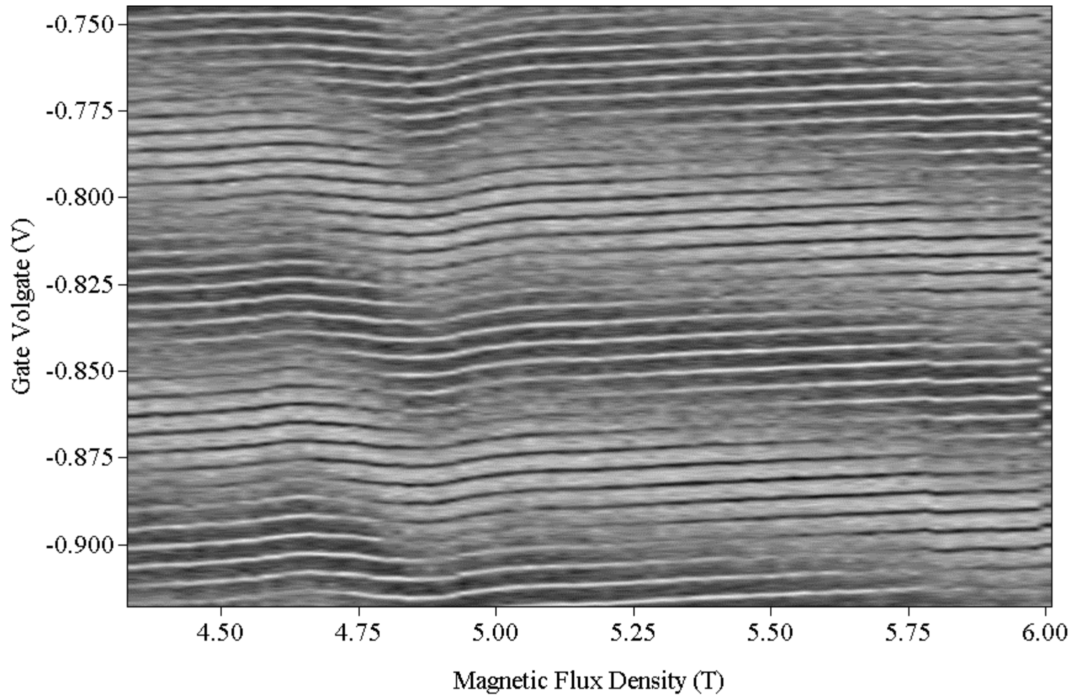


Figure 37. Effect of scanning the magnetic flux through the quantum dot on the gate voltage sweeps. The shade of the gray scale image corresponds to the magnitude of the AC signal through the SET. Light regions correspond to a high signal, while dark regions correspond to a small signal. The dip at a magnetic flux of 4.88T is probably due to the Landau level filling factor of ν=1.

value of $B_{\nu=1}$=4.88T could be considered realistic. On the other hand, the electron concentration in the quantum dot in all likelihood is lower than in the bulk, so the expected value of $B_{\nu=1}$ is lower than 4.14T. We examined the effect of the magnetic field over a wider range, and shows an example of the dependence of gate voltage scans.

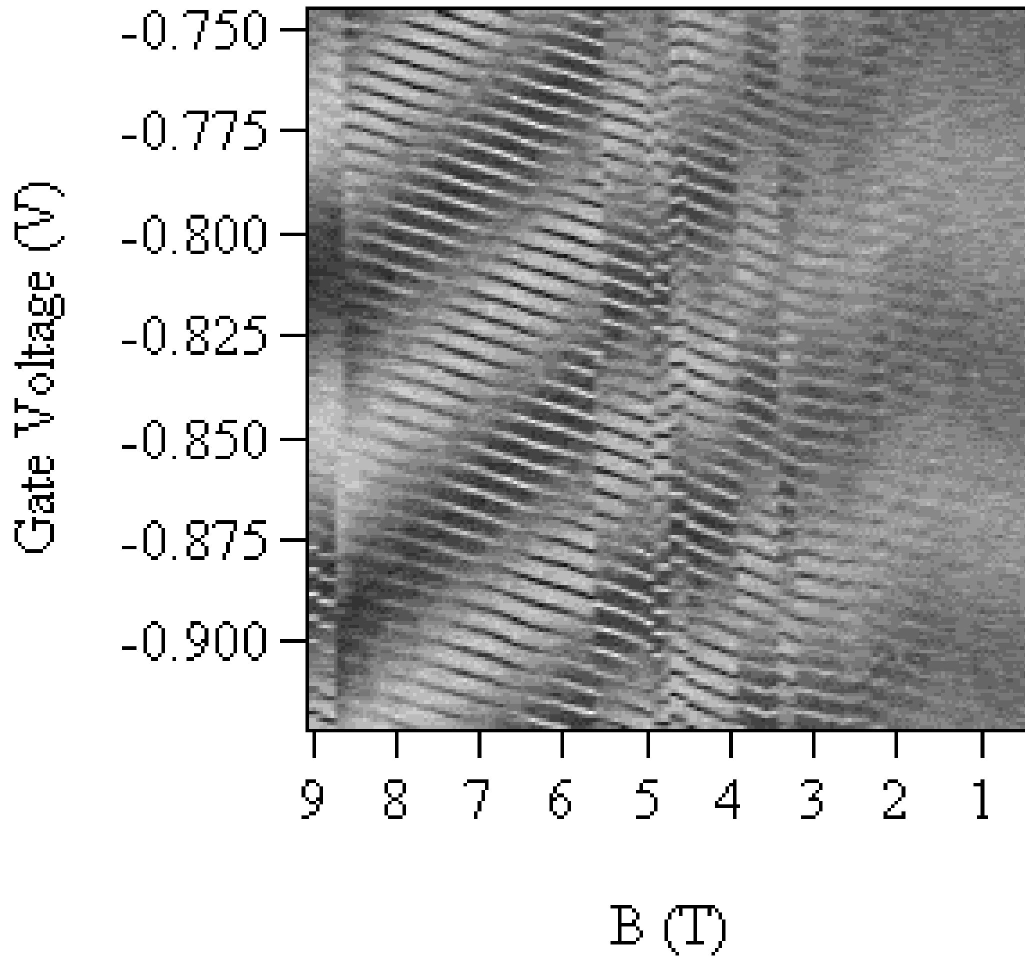


Figure 38. Dependence of gate voltage scans on magnetic flux density over a wide range of values. Light gray-high capacitance signal. Dark gray - low capacitance signal.

Figure 38 shows gate voltage scans over a range of magnetic flux density of 0.5T to 9T. Idenifying values of magnetic field corresponding to specific Landau level filling factors is rather difficult here for several reasons. One of the problems with performing gate voltage scans over such a wide range of magnetic field values is that the tunnel barrier conductance of the point contact coupling the quantum dot to the reservoir varies with magnetic field. For example, for B=9T, the tunnel barrier is quite high, so the quantization of charge on the quantum dot is quite strong. Here, the quantum dot capacitance peaks are fairly sharp, providing a good contrast in Figure 38. For small

values of magnetic field, the tunnel barriers are low, so the charge on the quantum dot becomes smeared. At magnetic flux density values of around 1T, it is very difficult to identify the traces corresponding to the quantum dot capacitance peaks. The fact that the tunnel barrier conductance changes with magnetic field means that the point contact voltage should be adjusted at different regions of magnetic field. Another problem in Figure 38 is that there are several charge fluctuation events. For example, at 5.6T and 8.7T, there are sharp boundaries in the figure. Here, there could have possibly been some charge traps that changed their state, and caused a discontinuous jump in the charge on the quantum dot and the central island of the SET. There are several such events in Figure 38, which make it very difficult to follow the development of a single quantum dot peak with magnetic field.

As mentioned before, the expected magnetic flux density at which $\nu=1$ in the quantum dot is 4.14T. Thus, we expect that $\nu=2$ at 2.07T. Figure 39 shows the gate voltage scans from 1.5T to 4.5T. It is difficult to identify a particular feature due to a change of filling factor in the quantum dot.

One of the motivations for performing the quantum dot capacitance measurements in magnetic field was to observe the variation of the compressibility of the quantum dot. We expected the introduction of magnetic field perpendicular to the plane of the quantum would create compressible and incompressible rings inside the dot [5-28]. By changing the magnitude of the magnetic field, it is possible to vary the area of these strips.

Consequently, the variation of the area of the quantum dot would create a capacitance signal through the SET. Unfortunately, we were not able to observe this effect.

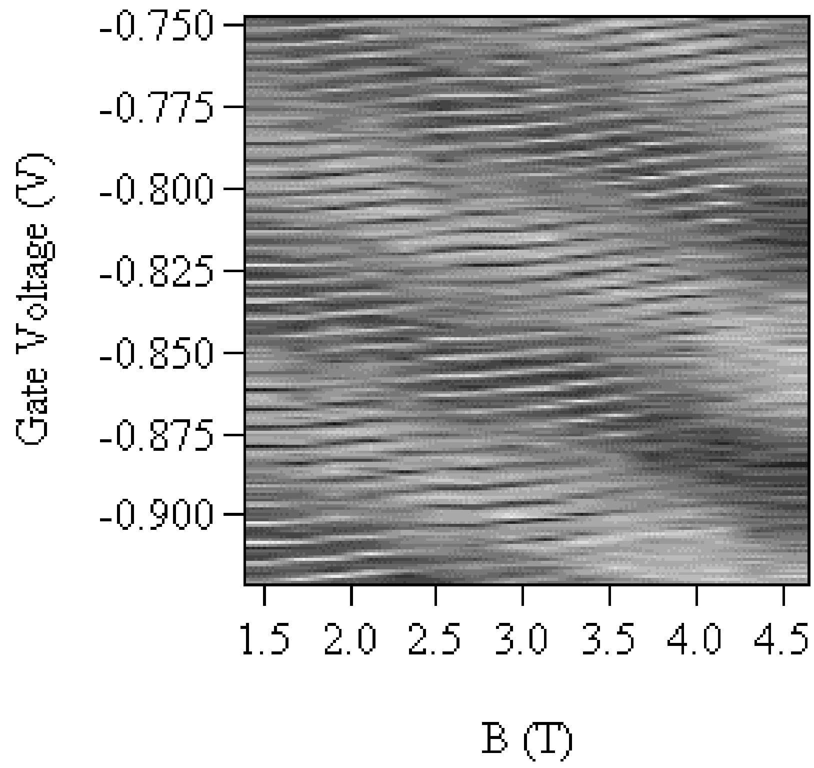


Figure 39. Dependence of gate voltage scans on magnetic flux density for small fields.

Chapter 6 Negative Screening

In some of our experiments with lateral quantum dot samples, such as depicted in Figure 21 of Chapter 5, we have observed some curious behavior for which we have not found a clear explanation. We named this phenomenon "negative screening". Here, as the name suggests, the screening of the AC potential in the system by electrons is opposite from what is expected.

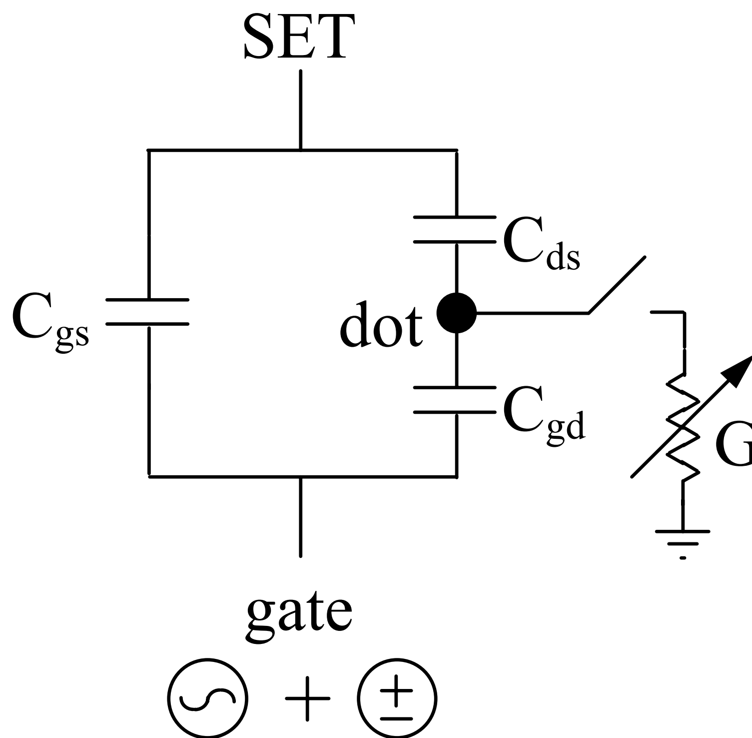


Figure 40. Schematic of the quantum dot experiment.

Figure 40 shows a schematic of the quantum dot experiment. A small AC voltage excitation is applied to the gate lead. The current through the SET is measured with a lock-in amplifier at the frequency of the excitation. The magnitude of the SET response

in the linear regime is proportional to the magnitude of the AC electric field reaching the central island of the SET. The top trace in Figure 41 shows an example of the dependence of the AC current through the SET as a function of the DC gate voltage. In this trace, there are periodically spaced peaks, with a average period of about 6.3mV. These peaks correspond to electrons tunneling onto the quantum dot. There is also an overall envelope modulation of the signal with a period of about 94mV. This modulation arises from the direct capacitive coupling from the gate to the central island of the SET.

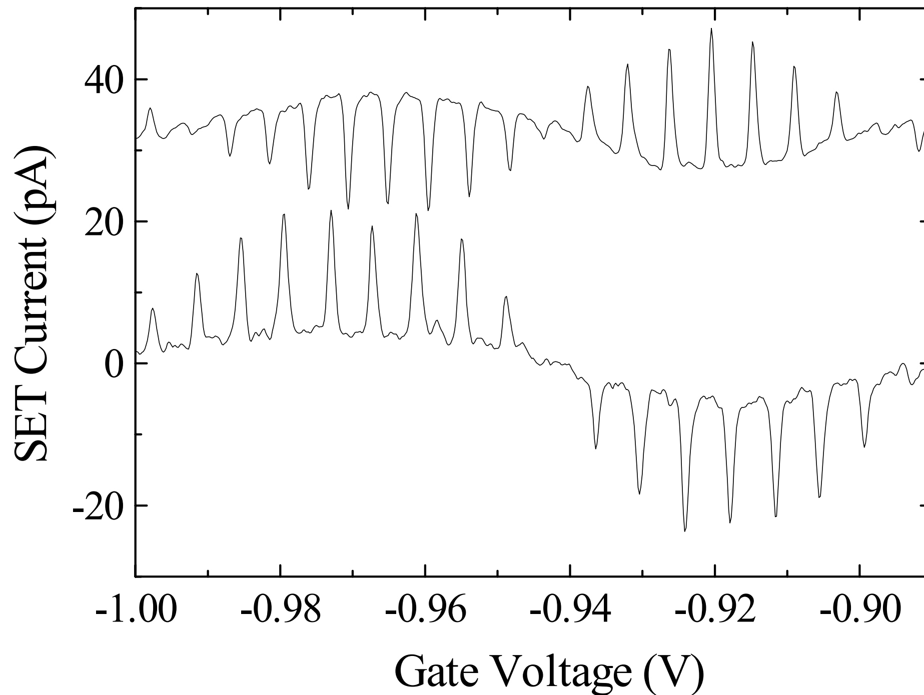


Figure 41. Example of negative screening in a lateral quantum dot. Top: regular positive screening observed in all samples. Offset by +32pA for clarity. Bottom: negative screening observed in the high tunnel barrier resistance regime only in a few samples. Both traces were performed at a refrigerator temperature of 0.050K.

Under normal operating conditions, the electrons tunnel onto the dot from the grounded reservoir through the tunnel barrier, denoted as “G” in Figure 40. Because the quantum dot operates on the Coulomb blockade principle, electrons can tunnel onto the dot only around certain values of gate voltage. These values correspond to the periodically spaced peaks in the top plot of Figure 41. Between these peaks, the dot potential is essentially electrically “floating”, because no charge is allowed to flow between it and the reservoir. At values of gate voltage where tunneling of electrons onto the quantum dot is permitted, the dot potential is equilibrated with the grounded reservoir by the electrons tunneling onto the dot. At these points, the effect of the equilibrating of the potential of the quantum dot is similar to the effect of placing a grounded metal sheet between the gate and the SET. Here, the quantum dot is an effective screen of the AC potential and it shields most of the AC electric field lines from reaching the SET central island. By shielding the AC field, the screening effect of the quantum dot tends to reduce the SET signal to zero. In fact, in the top trace of Figure 41, there is actually an overshoot of the screening of the SET signal past zero. This “overscreening” is due to the fact that charge must flow as discrete electrons, and they make up for not screening between peaks by overscreening at the peak centers.

In addition to usual screening behavior described above which appears in all quantum dot samples, we have observed “negative screening” in some of the samples. “Negative screening” suggests that the quantum dot screens the AC electric field in an opposite manner from what is expected. Here, rather than decreasing the AC field reaching the SET, the electrons tunneling onto the quantum dot increase it, as shown in the bottom

trace of Figure 41. In this trace, the peaks corresponding to electrons tunneling onto the quantum dot point in a direction that increases the overall SET signal. Thus suggests that electrons tunnel into and out of the dot 180° out of phase compared to the expected response.

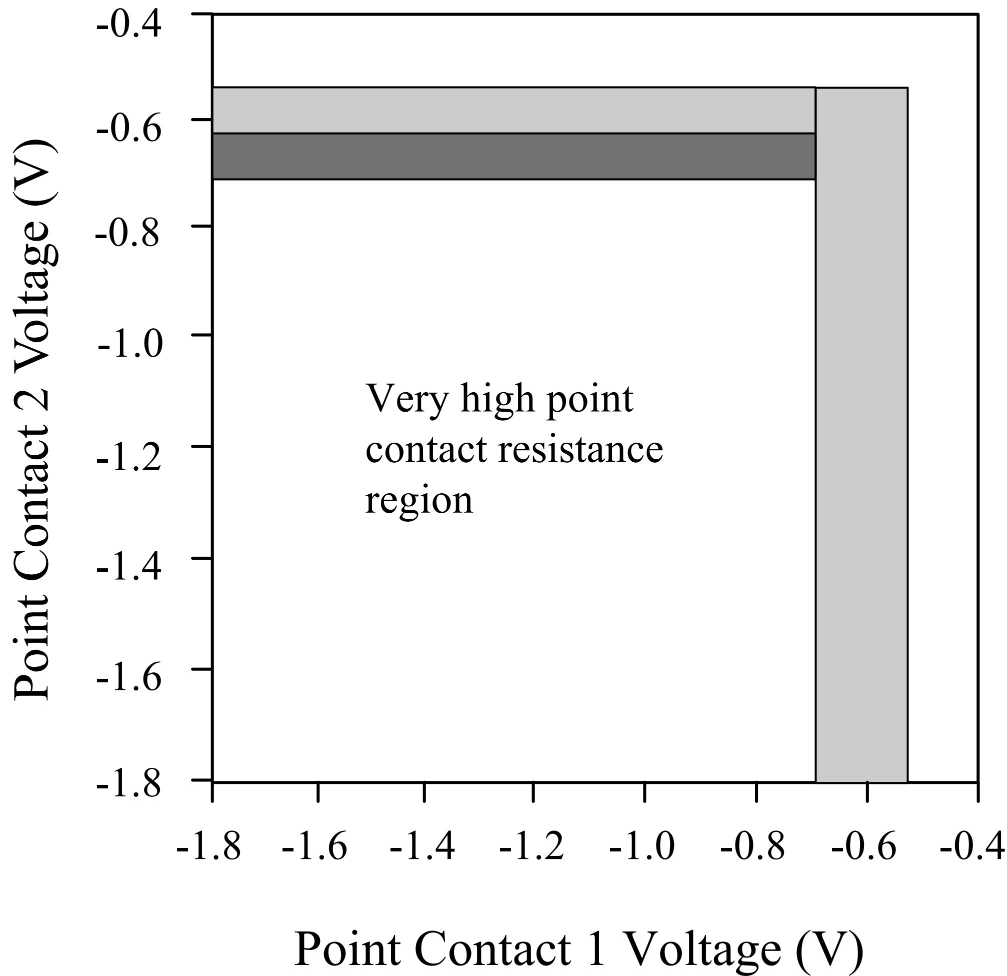


Figure 42. Phase diagram of the single-electron peaks of the quantum dot. Light gray areas: usual positive screening characteristics. Dark gray: negative screening peaks. White area: absence of single-electron peaks.

The character of the "negative screening" effect is entirely different from the usual behavior of the quantum dot. Here, rather than separating the gate from the SET, the electrons tunneling onto the dot seem to increase the coupling between the gate and the central island. We have observed this "negative screening" behavior only in a few of the quantum dot samples. These samples display "negative screening" for electrons tunneling only through specific point contacts. In addition, this effect appears for very high tunnel barrier resistance values (R_T>1GΩ).

Figure 42 shows a phase diagram of the screening characteristics in one of our quantum dot samples. In this figure, the light gray areas correspond to the usual positive screening quantum dot peaks displayed in the top trace of Figure 41. Dark gray areas correspond to negative screening peaks as in the bottom trace of Figure 41. Clearly, the effect of the different point contact on the presence of negative screening is not symmetric. Negative screening is only present for electrons tunneling across point contact 2, while there is no negative screening peaks for electrons tunneling across point contact 1. In addition, the negative screening peaks appear for a relatively large negative bias of point contact 2. For example, if the tunneling across point contact 1 is completely suppressed by biasing it at -1.2V relative to the 2DEG, then as the voltage on point contact 2 is varied, the following occurs. For point contact 2 voltage biases more positive than -0.54V, no quantum dot single-electron peaks are present. This happens because the tunnel barrier resistance of point contact 2 is lower than $\frac{h}{2e^2} = 12.9\text{k}\Omega$, and the charge quantization is destroyed. As point contact 2 voltage is made more negative than -0.54V, usual positive screening single-electron peaks appear in gate voltage sweeps. Then, as point contact 2 voltage is made more negative than -0.62V, the single-electron peaks change their orientation, and negative screening appears. At this value of point contact 2 voltage bias, we expect that the tunnel barrier resistance is quite high, on the order of 100GΩ. For values of point contact 2 voltage bias more negative than -0.7V, the quantum dot single-electron peaks disappear altogether. Here, the $R_T C_\Sigma$ time of charging the quantum dot with a single electron is longer than the period of the AC signal. The period of the AC

signal is 1ms (f=1kHz). The total capacitance of the quantum dot is: $C_{\Sigma} = 340\text{aF}$, which leads to a tunnel resistance of about $R_T = 3\text{T}\Omega$ at the point of disappearance of the quantum dot peaks.

Figure 43 supports the above description. In Figure 43a, for point contact voltage of -0.57V, the quantum dot single-electron peaks appear in the usual positive screening orientation. Also, at this point contact voltage bias, the quadrature, or the 90° out-of-phase signal due to the single-electrons tunneling onto the quantum dot is very small, as shown in Figure 44a. Figure 43b shows that for a point contact 2 voltage of -0.63V, the usual screening single-electron peaks are being replaced by “negative screening” peaks. At this point, the quadrature signal from the quantum dot single electrons is quite high, as shown in Figure 44b. More negative values of point contact 2 voltage bias increase the “negative screening” peaks, as shown in Figure 43c, and the quadrature component is reduced to zero, as in Figure 44c.

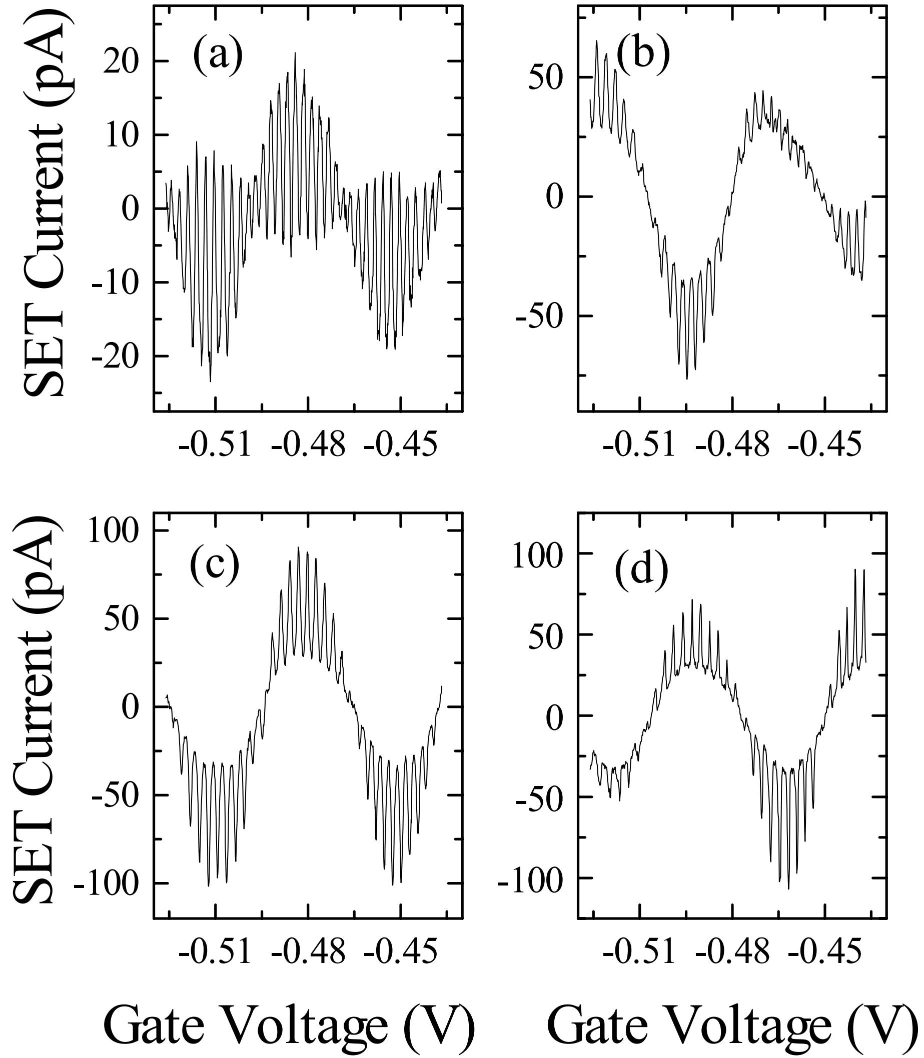


Figure 43. The dependence of the quantum dot single-electron peaks on the voltage on the lead defining point contact 2. Each trace represents the in-phase output signal of the lock-in amplifier for a different point contact 2 voltage. (a) -0.57V (b) -0.63V (c) -0. 67V (d) -0.69V.

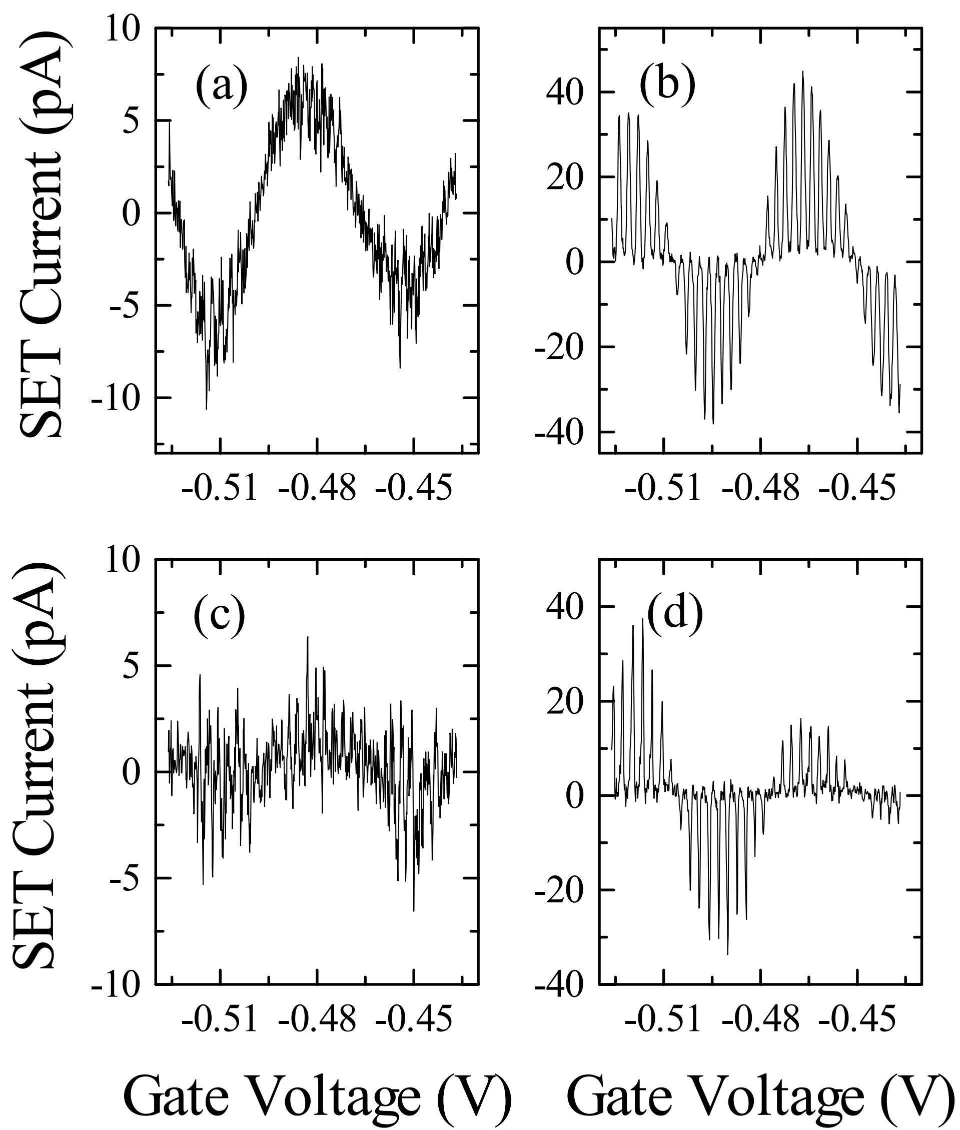


Figure 44. Dependence of the quadrature signal of of the lock-in amplifer on the voltage on the lead defining point contact 2. (a) -0.57V (b) -0.63V (c) -0.67V (d) -0.69V.

Finally, for point contact 2 voltage bias of -0.69V, the "negative screening" peaks begin to disappear, as in Figure 43d, and the phase of the signal rotates, as evident by the large quadrature signal in Figure 44d.

If one were to completely believe the "negative screening" results that we have described above, then it would seem that we have observed something quite extraordinary - the tunneling of electron-like particles that have positive charge. Of course, the prospect of such a discovery would be quite exciting, it is quite improbable, so we turned to more ordinary physical origins for the explanation of this effect.

It is difficult to completely explain the "negative screening" phenomenon. Nevertheless, there are several clues that may lead to a possible description. First, we turn to the fact that the negative screening peaks only appear for extremely high tunnel barrier resistances, on the order of 100GΩ. This range of resistance is on the scale of possible leakage, which raises a certain suspicion. Also, we have observed "negative screening" only in a few of the samples, and only for tunneling through certain point contacts in these samples. This suggests that "negative screening" is a sample-dependent phenomenon, rather than some general property of electron tunneling through point contact tunnel barriers. So, even through it is difficult to imagine a scenario, in which leakage can produce an effect such as "negative screening", the above stated facts seem to point in this direction.

Chapter 7 Conclusion

In this thesis, we demonstrated that the extremely high charge sensitivity of the single-electron transistor makes it useful for various charge detection applications. We have described the implementation of an aluminum single-electron transistor (SET) as an ultrasensitive detector in charge measurement experiments on semiconductor quantum dots. The double-angle evaporation technique was used to reliably fabricate the aluminum SETs on semiconductor samples. In one of the experiments, the SET was used to measure the charge quantization on the quantum dot while varying the strength of the coupling between the dot and the leads. With standard measurement techniques, we were able to obtain a sensitivity of $1.2 \times 10^{-3} \frac{e}{\sqrt{\mathrm{Hz}}}$ to charge on the quantum dot in that experiment. This charge sensitivity allowed us to perform a careful study of the effect of increased coupling strength between the quantum dot and the environment on the broadening of the energy levels on the dot, as described in Chapter 5.

In the quantum dot measurements, we found that the level broadening on the quantum dot cannot be described by a Lorentzian broadening function [7-7-1] nor by a renormalized charging energy [7-2]. Rather, the proper theoretical approach to this problem is through calculations based on perturbation theory [7-3][7-4], to which we compared our data.

There are some possible extensions of this thesis for future work:

- Spin-polarized state. During the experiments of sensing charge on the quantum dot, one of the motivations for performing measurements in a magnetic field was to observe the transition of the system with unfavored spin to one where the spins of all the electrons are parallel. Here, theoretical calculations predict that the lineshape has a cosine shape [7-4]. We were not able to observe this spin-polarized state, and it would be very interesting to verify the theoretical prediction.
- Compressibility. The charge sensitivity of the SET allows one not only to detect electrons tunneling on and off the quantum dot, but to detect changes in the shape of the dot. In magnetic field, compressible and incompressible strips develop in the quantum dot, because the electron concentration is not uniform across the entire area of the dot. The concentration is maximum at the center, and it falls off to zero at the edges of the dot. As the magnetic field is varied, these strips move, and the metallic, or compressible strips change their size and location. The SET can detect these changes and can be used to study the physics of these compressible and incompressible strips.
- Composite fermions. Theory predicts that at certain large values of magnetic field, there are quasi-particles in a 2DEG, called composite fermions, that behave as electrons do for a zero magnetic field [7-5]. The composite fermions appear in a regime, referred to as the Fractional Quantum Hall regime [7-6]. Composite fermions have charge of $e/3$, where e is the charge of an electron. It would be interesting to perform the charge detection experiment on a quantum dot in the Fractional Quantum Hall regime and measure whether the physics of Coulomb blockade takes composite fermions into account, or whether it is still based on regular electrons. This can be

observed by determining if the period between the capacitance peaks changes from e/C_g to $e/3C_g$.

- Charge sensing applications. The extremely high charge sensitivity of the SET can be applied to a wide range of applications. For example: a data storage paradigm can be conceived where a read head with a SET as the sensor is used to read the data stored on a rotating disk. The information can be stored in the form of small packets of charge in elements, such as quantum dots. Of course, to be useful, the SET must be fabricated with dimensions on the order of 1-2nm, so that it operates at room temperature.

Appendix A Fabrication Recipes

Most of the processing steps described below have been performed in the Nanostructures Laboratory at MIT, except for the photolithography and the electron-beam lithography steps.

1. Cleaning

The cleanliness of the substrate is extremely important for the success of the subsequent processing steps, so the following procedure is performed on all GaAs samples, both after receipt from the grower, and before every major step in the process.

a. Rinse the samples in deionized (DI) water for 1minute.

b. Blow dry with pressurized N_2 gun.

c. Place the samples in a Teflon basket with holes in the bottom.

d. Boil in 1,1,1 Trichloroethane (TCA) for 10 minutes.

e. Ultrasonic clean in acetone for 10 minutes. The Teflon basket prevents the brittle GaAs samples from hitting against the walls of the glass beaker during the ultrasonic bath.

f. Ultrasonic clean in methanol for 10 minutes.

g. Quickly blow dry with N_2 gun. If the methanol dries by itself, streaks form on the surface of the substrate.

h. The substrate surface should be clean now. The surface must be covered with photoresist or electron-beam resist, depending on the next processing step, as soon as possible after drying.

2. Photolithography

After the samples have been cleaned as described above, photoresist is applied to the surface to prepare the samples for photolithography. The initial processing steps involve relatively large features (greater than about 5μm), so ordinary photolithography techniques will suffice.

a. Spin Shipley 1813 photoresist at 4500 RPM for 45 seconds.

b. Bake for 30 minutes in a 90°C oven. The resulting thickness of the photoresist film is about 1.1μm.

c. The samples must be stored in a lightproof container for transport to the building 13 Microlab facility for photo exposure.

d. Exposure is performed in a Karl Suss aligner. The exposure time is generally 8-15 seconds, but it must be calibrated at the beginning of the day, because the power output of the lamp fluctuates quite a lot. The most difficult part in the photolithography procedure is the proper alignment of the pattern. The first layer, the mesa definition, must be as parallel as possible to the crystallographic orientation of the wafer. Each chip contains 9 or 18 mesas. After all the photolithography steps, each chip will be cleaved into individual mesas for electron-beam lithography, so it is very desirable that the crystal axes run parallel to the mesa edges.

e. Develop by spraying with CD-30 developer for 30 seconds. The pattern should start clearing after about 15 seconds. The exposure should be calibrated so that the pattern is properly developed after 30 seconds. In the absence of CD-30 developer, MF319 developer can be used.

f. Rinse in DI water for 1 minute.

For photoresist patterns for metal evaporation and liftoff, sometimes it is beneficial to perform a slightly different development procedure to generate a small undercut in the resist profile. Generally, vertical sidewalls are sufficient for liftoff when the evaporation is performed with a point source. Nevertheless, under certain conditions, such as aging photoresist, the profile may be slightly overcut, so just as a precaution, we perform the following procedure to create an undercut.

e. Soak in Chlorobenzene for 4 minutes.

f. Bake the sample for 4 minutes in a 90C oven.

g. Develop by spraying CD-30 developer for 30 seconds. Because of the Chlorobenzene soak, the exposure time must be increased to about 15-17 seconds to properly develop the samples in 30 seconds.

h. Rinse in water for 1 minute.

3. Mesa definition

The main consideration in the definition of the mesas in GaAs samples is that most wet etching solutions are anisotropic. Depending on the crystallographic orientation, the etched edge may have an undercut profile, or the opposite,

overcut profile. We found that the H_2SO_4 based etching solution gives the best results.

a. Etch the mesa in H_2SO_4:H_2O_2:H_2O (1:8:1000) solution. The etch rate of GaAs in this solution is about 43nm/min, but it should be calibrated before every important run.

b. Rinse in water for about 1 minute to stop the etch.

c. Strip the photoresist by soaking in acetone for about 1-2 minutes. Make sure that all the photoresist is gone, especially at the corners of the chip, where it builds up after spinning.

d. Rinse in methanol for a few seconds. It is very important that methanol is applied immediately to the chip after it is removed from the acetone bath. If the acetone dries before methanol is applied, it leaves residue which is very difficult to remove.

e. Blow dry with N_2.

f. Spin and bake photoresist as described above for the next step.

4. Ohmic contacts

The contacts to the Two-Dimensional Electron Gas (2DEG) in the GaAs heterostructure are deposited by electron-beam evaporation onto the sample surface through a pattern defined in photoresist. The exposure and development are performed using chlorobenzene for liftoff as in the procedure described above. Before being loaded into the evaporator, the following procedure is performed:

a. UV ozone clean for 30 seconds.

b. Rinse in water for 1 minute.

c. Blow dry with N_2.

d. Etch in H_2SO_4:H_2O_2:H_2O (1:8:1000) solution for 15 seconds.

e. Blow dry with N_2.

The metal evaporation is performed at a pressure of approximately 4×10^{-7} Torr at a rate of 0.5 nm/s. The chamber is cleaned before loading the samples.

f. Evaporate:

Nickel - 10 nm

Germanium - 35 nm

Gold - 70 nm

g. Liftoff the unwanted metal by soaking in acetone. This is a rather tricky procedure. The success of liftoff depends on several factors: the proper profile of the resist, the size of the molten area in the source of the evaporator (as close to a point source as possible). The endpoint of liftoff is usually determined from the appearance of the surface of the metal. The surface of a properly performed evaporation will become rough a few seconds after being placed in acetone. This indicates that acetone has begun to dissolve the photoresist under the metal. Within a few minutes, depending on the degree of undercut, amount of evaporated metal, thickness of the resist, etc., the metal surface becomes smooth and shiny again. At this point, photoresist is completely dissolved and the metal has "lifted off" the surface of the wafer.

h. Spray with acetone immediately after removing the sample from the acetone bath. Here, as described above, acetone must not be allowed to dry on the substrate surface.

i. Spray with methanol. This is the last chance to remove any loose particles of metal from the surface of the substrate. After the substrate is dry, there is virtually no chance of removing metal particles that stuck to the surface. Really make sure that the surface is clean.

j. Blow dry with N_2.

After successful liftoff procedure, the ohmic contacts are annealed. This procedure diffuses the metal eutectic into the substrate, creating a contact to the 2DEG that has a resistive, rather than a diode-like characteristic.

k. Anneal the contacts at 425°C for 0.7min. The parameters for the Eurotherm strip heater that was used for the ohmic contacts are:

Pr1: 400	Pr2: 600	Pr3: 100	Pr4: 800
Pl1: 200	Pl2: 410	Pl3: 425	Pl4: 0
Pd1: 0.5	Pd2: 0	Pd3: 0.7	Pd4: End

l. Check the resistance of the ohmic contacts on the probe station.

m. Clean the substrates and spin and bake the photoresist as described above.

5. Gold leads

The pattern for this photolithography step contains the smallest features (~5μm) of all the photolithography steps, which makes it the most difficult one. The exposure must be well-aligned. The sample must be pressed very evenly against the mask during exposure, which is difficult with large photoresist build-up at the corners of the chip. The exposure must be properly selected not to over- or underdevelop the fine features. The development is performed with chlorobenzene, as described above, to ensure good liftoff. Before being loaded

into the evaporator, the samples are subjected to a 30 second clean in UV ozone. The metal is evaporated in the electron-beam evaporator with 5nm of titanium or chrome as the adhesion layer and about 120-150 nm of gold.

Liftoff is performed in acetone as described above. To speed up the liftoff procedure, the sample can be placed in an ultrasonic bath. If the acetone does not seem to be dissolving the photoresist, the sample can be placed in a boiling 1-methyl-pyrrolidone (NMP). Boiling NMP is a rather extreme measure, so great care must be taken.

6. Electron beam resist preparation

Now that the substrates have been through all the photolithography steps and cleaned, the resist for electron-beam lithography can be applied with the following procedure:

a. Spin Methacrylic acid (MAA) copolymer 11% in ethyl lactate at 5000 RPM for 45 seconds. The resulting film thickness is about 450nm.

b. Bake in an oven at 125°C for 30 minutes.

c. Flood expose in the OAI aligner with λ=220nm mirrors for 200 seconds. The power density of the lamp should be about 1mW/cm^2. This step is performed to introduce a certain dose to the bottom layer of the resist and increase the degree of undercut for the double-angle evaporation, as described in the Fabrication chapter.

d. Spin 950K molecular weight poly-methyl-methacrylate (PMMA) dissolved 2% in Anisole at 5000 RPM for 45 seconds. The resulting film thickness is about 50nm.

7. Electron-beam lithography

The electron-beam lithography is performed in a JEOL 6400 scanning-electron microscope. The beam parameters for the lithography are:

Accelerating voltage: 40kV. This is the maximum voltage of the machine.

Higher voltage means that the effect of backscattering is smaller.

Probe current: 20pA. Smaller probe current would increase the resolution, but the poor signal-to-noise ratio makes the focusing virtually impossible.

Aperture setting: 4. Smallest aperture is necessary for the small probe current.

Working distance: 6mm. Getting the sample as close as possible to the gun is necessary for good resolution.

Magnification: 1000. All the patterns are written with a magnification of 1000.

Obviously, the magnification can and should be changed during the set-up and optimization of the beam.

Before writing, the microscope beam must be properly aligned, focused, corrected for astigmatism, etc. This is performed on a resolution standard, placed in the microscope chamber next to the sample on the chip holder. The resolution standard is made of a thin film of gold on a graphite substrate. The gold consists of balls of diameters ranging from 50nm to 100nm and can easily be used for

focusing at a magnification of 300,000, the maximum magnification of the machine. The beam alignment is performed in the following procedure:

a. Slowly ramp the probe current up to about 240μA. This should take a few minutes, so that the filament does not suffer from thermal shock. If the microscope is in line scan mode, the line should increase up to a certain maximum value, then decrease, and finally increase and saturate at a probe current of approximately 240μA. This should be performed at a magnification less than 1000.
b. Align the electron gun. Maximize the secondary electron signal by shifting and tilting the gun in the x and y directions. The optimum gun position can be obtained after several iterations. After the gun is properly aligned, the microscope can be switched to TV scan mode.
c. At a magnification of about 10,000, focus on the resolution standard. If that proves impossible, it is probably due to extreme astigmatism. Reduce the magnification and try to adjust the x and y astigmatism controls.
d. Align the aperture by using the wobbler, which moves the plane of focus up and down. With a properly aligned aperture, the image should defocus uniformly in all directions, or "breathe". If the image is moving up and down or sideways, the aperture needs to be moved in the same direction. The focus may need to be changed afterwards.
e. Increase the magnification to 100,000-300,000. Adjust the astigmatism. Improper astigmatism results in an elliptical beam spot. The effect can be

seen by the appearance of diagonal striations in the image if the focus is slightly changed. For severe astigmatism, these striations prevent one from resolving the image at large magnifications.

f. At this point, the lens should be cleared of any electrically charged particles. Here, the electric field of the lens is turned off, and any charged particles are pumped away. If this process results in any change in the image, such as a positional shift, change of focus, the aperture and the astigmatism corrections need to be repeated and the lens should be cleared again. This process should be repeated several times, until there is no change in the image after clearing the lens.

g. Now, the beam is properly aligned, and it is ready for writing. Move a corner of the sample into view. Use the fine height adjustment to bring the surface of the sample into the plane of focus. This should be done at a magnification of about 1000 or higher.

h. Find the corner of the gold leads and use the line scan mode to quickly focus on the edge of the lead at a magnification of about 40,000.

i. Find the center of the writing field. In our mask, we have a gold spot of about 5μm in diameter for this purpose. Use the Faraday cup to fine tune the probe current to 20pA, if it has changed.

j. Use the line scan mode again to do a final focus on the edge of the gold spot.

k. Turn the control of the beam over to the computer and write the pattern.

After writing, the sample is removed from the microscope chamber. The pattern is developed as following:

l. Soak in a solution of MIBK:IPA 2:3 for 60 seconds. The developer should be continuously swirled for the entire development time.

m. Soak in IPA for 30 seconds.

n. Blow dry with N_2.

8. SET evaporation

The samples are subjected to a 3-4 second oxygen plasma ashing immediately before being loaded into the evaporator. This process eliminates any thin film of residue that remains after the development. It is very important to remove this residue film, because it prevents good electrical contact to the lower metal layer. The evaporation of the SET devices is performed in an electron-beam evaporator, at a pressure of about 4×10^{-7} Torr.

a. Evaporate 30 nm of aluminum at a rate of 0.5 nm/s. The angle of the sample stage is -9°.

b. Wait 10 minutes for cooldown.

c. Close the High-Vac valve.

d. Introduce 50-100mTorr of oxygen into the chamber.

e. Oxidize for 10 minutes.

f. Pump the oxygen away by opening the High-Vac valve. Wait until the pressure falls into the 10^{-7} Torr range.

g. Evaporate 35 nm of aluminum at a rate of 0.5 nm/s. The angle of the sample stage is +9°.

h. Wait 10 minutes for cooldown.

i. Remove the sample from the evaporator.

Now that the sample holds single-electron transistors, handling of the sample must be very careful, because these devices are very susceptible to damage from static discharge. Liftoff is performed by soaking in acetone. Since the profile of the pattern in the resist has a large undercut, liftoff is very quick and easy. Spray with methanol while the sample is still wet with acetone and blow dry with N_2. The sample should be placed in a static protective container.

9. Bonding

The static-sensitive SETs are protected from the moment when they are evaporated by a gold wire that shorts all the bonding pads in the gold leads optical layer. As the sample is mounted on the cryogenic probe, these shorting wires must be scratched with a scriber. Since the SETs must be protected at all times, these shorting wires are scratched only after other shorting wires are bonded between the bonding pads. When the header with the sample is mounted on the cryogenic probe, the shorting wires that have been bonded on can be easily removed with tweezers. The cryogenic probe has a breakout box with switches that keep the sample grounded when it is not connected to measurement equipment.

Appendix B Point Contacts

During the development of the experiment described in Chapter 5, we have measured many different samples. One of the structures that we used is depicted in the micrograph in Figure B45. This micrograph shows a structure nearly identical to the one pictured in Figure 21 in Chapter 5 with one major difference.

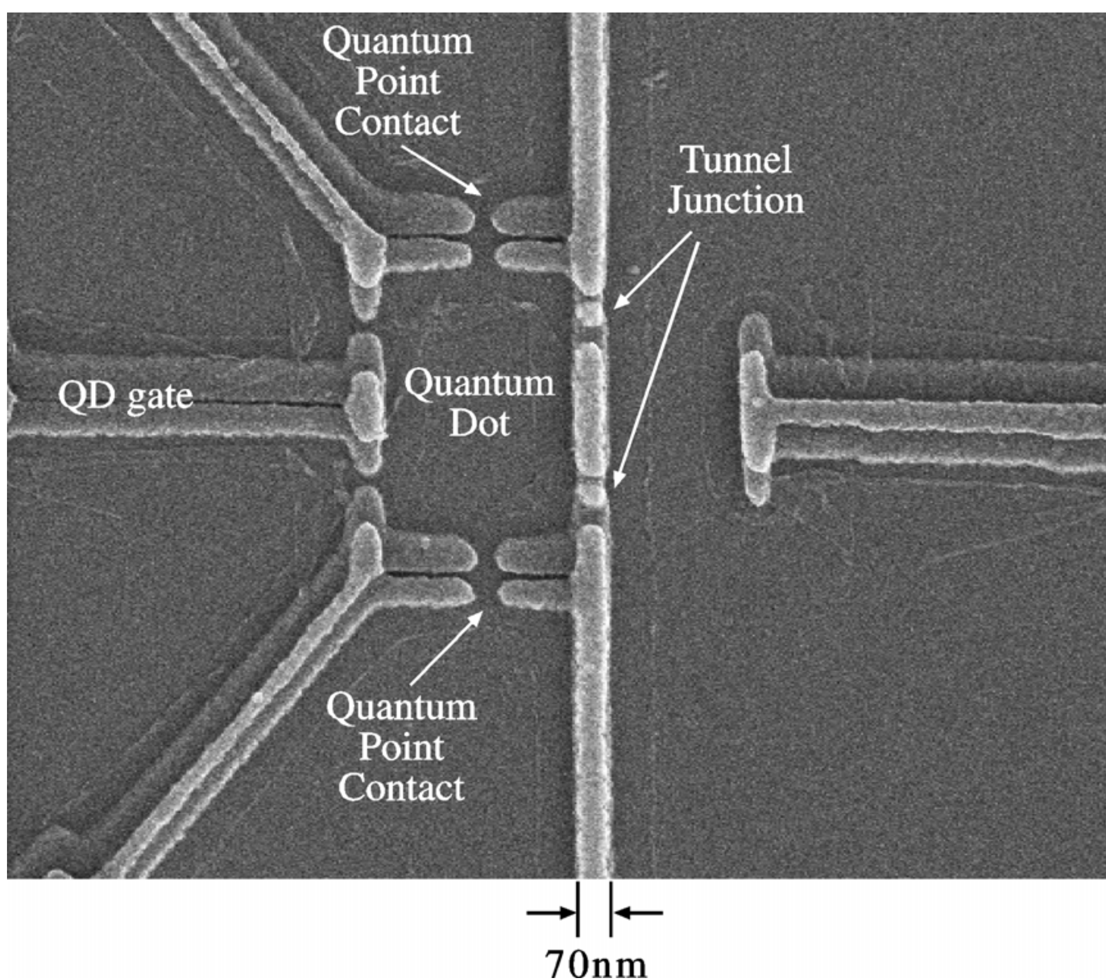


Figure B45. Micrograph of a lateral quantum dot sample with double quantum point contacts.

The technique of double-angle evaporation described in Chapter 2 results in a shadow effect, or a "doubling" of features oriented parallel to the tilting axis of the sample. This "doubling" is clear in the leads defining the point contacts in Figure B45. It turns out that the characteristics of the point contacts defined in this manner are significantly affected by the shape of the leads. Properly defined point contacts create electrostatic potentials in the 2DEG that meet in a small point. In other words, the electrons tunneling across the point contact from one section of the 2DEG to another must do so only at one particular point in the sample, and the tunneling distance must also be very small. The point contacts in the sample shown in Figure B45 constrict the electron tunneling to a very

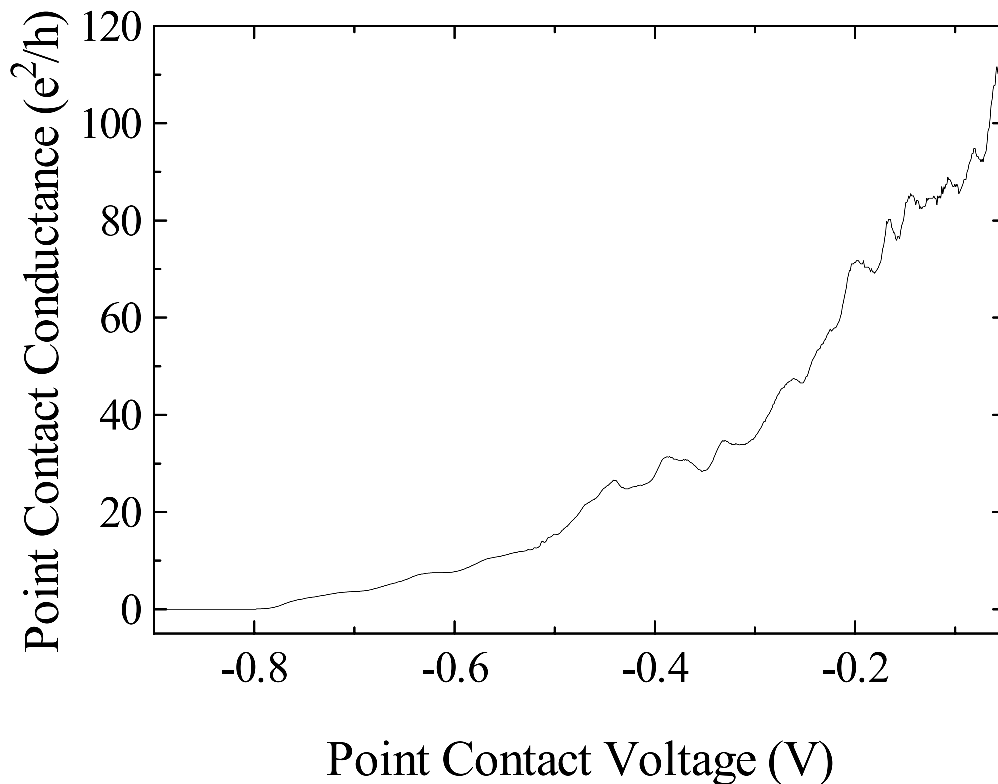


Figure B46. Conductance through point contacts defined as shown in Figure B45.

narrow region, but the distance across which the electrons must tunnel is too long because of the lead "doubling" caused by the double-angle evaporation. An example of the conductance of such point contacts is shown in Figure B46. Here, the familiar steps of $2e^2/h$, due to individual conductance channels are missing: the tunnel barrier conductance falls off fairly smoothly with voltage on the lead.

In the experiments on quantum fluctuations described in Chapter 5, we measured the changes in the capacitance lineshape of the quantum dot as we changed the tunnel barrier conductance. In comparing the resulting lineshapes to theoretical calculations, we used values for the tunnel barrier conductance that we extrapolated from the observation of the shifts in the conductance plateaus of the point contact for a completely open quantum dot. Clearly, a point contact without these conductance plateaus makes this comparison to the theoretical calculations very difficult. To solve this problem, we shifted the leads defining the point contacts to account for the "doubling" created by the double-angle evaporation method and created true point contacts, depicted in Figure 21 of Chapter 5.

Appendix C MATLAB program for SET current-voltage characteristics simulation

```
% iv.m
%       This Matlab program calculates the current through an SET as a function of
%       source-drain voltage, V, for a given gate voltage, Vg.  This program is called
%       from Matlab by changing to the directory of the program and typing 'iv' at the
%       Matlab command prompt.  The gate Voltage, Vg, is defined in the Matlab
%       environment before calling the program.  The first few lines of the program
%       define the operating temperature (in K), and both capacitances and resistances of
%       the SET.  These parameters can be changed by simply editing the file and saving
%       it.  The capacitances are defined in Farads, and resistances in ohms.  This
%       program outputs a plot which is generated by the command 'plot(V,I)'.  Both
%       V and I are vectors.  The current is calculated from the tunneling rate equations
%       as in [C-1].
k=1.38e-23;                 % Boltzmann's constant
T=.05;                      % Temperature in Kelvin
e=1.602e-19;                % Charge of an electron in Coulombs
C1=80e-18;                  % Capacitance of tunnel junction 1 in farads
C2=80e-18;                  % Capacitance of tunnel junction 2 in farads
Cg=40e-18;                  % Gate capacitance in farads
Csum=C1+C2+Cg;              % Total capacitance of the central island
Ec=(e^2)/(2*Csum);          % Charging energy
R1=0.475e6;                 % Resistance of tunnel junction 1 in ohms
R2=0.475e6;                 % Resistance of tunnel junction 2 in ohms
V=[-1000:1000];             % Vector for the source-drain voltage
V=V*2e-6;                   % V goes from -2mV to +2mV
V=V+eps;                    % Avoid dividing by zero
N=[-8:8];
n=length(N);
Nt=N'*ones(size(V));
Vt=ones(size(N))'*V;
V1=(Vt*(C2/Csum))-(Nt*e/Csum)+(Vg*(Cg/Csum));
V2=(Vt*(C1+Cg)/Csum)+(Nt*e/Csum)-(Vg*(Cg/Csum));
p1=1/(e^2*R1);
p2=1/(e^2*R2);
DEr1=(V1*e)-Ec;
DEl1=(-V1*e)-Ec;
DEr2=(V2*e)-Ec;
DEl2=(-V2*e)-Ec;
```

```
r1=p1*DEr1./(1-exp(-DEr1/(k*T)));
l1=p1*DEl1./(1-exp(-DEl1/(k*T)));
l2=p2*DEl2./(1-exp(-DEl2/(k*T)));
r2=p2*DEr2./(1-exp(-DEr2/(k*T)));
x=r1+l2;
y=l1+r2;
prodxl=x;
prodyu=y;
prodxl(1,:)=ones(size(V));
prodyu(n,:)=ones(size(V));
for i=1:n-1,
 prodxl(i+1,:)=prodxl(i,:).*x(i,:);
 prodyu(n-i,:)=prodyu(n-i+1,:).*y(n-i+1,:);
end
ro=prodxl.*prodyu;
sro=sum(ro);
for i=1:length(V),
 ro(:,i)=ro(:,i)/sro(i);
end
I=-e*sum((l2-r2).*ro);                          % Total current through the SET
plot(V,I,'w')
```

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